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(54) **MEMORY CELLS, METHODS OF FORMING MEMORY CELLS, AND METHODS OF PROGRAMMING MEMORY CELLS**

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,715,685	A	12/1987	Yaniv et al.
4,964,080	A	10/1990	Tzeng

(Continued)

FOREIGN PATENT DOCUMENTS

CN	1339159	3/2002
CN	1444284	9/2003

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 12/701,885, filed Feb. 8, 2010, Sandhu et al.

(Continued)

Primary Examiner — Harry W Byrne
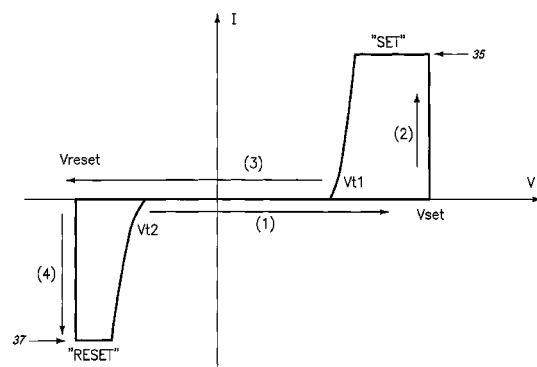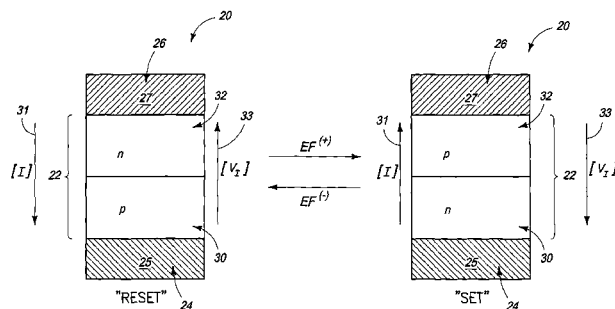(74) *Attorney, Agent, or Firm* — Wells St. John P.S.

(57) **ABSTRACT**

Some embodiments include methods in which a memory cell is formed to have programmable material between first and second access lines, with the programmable material having two compositionally different regions. A concentration of ions and/or ion-vacancies may be altered in at least one of the regions to change a memory state of the memory cell and to simultaneously form a pn diode. Some embodiments include memory cells having programmable material with two compositionally different regions, and having ions and/or ion-vacancies diffusible into at least one of the regions. The memory cell has a memory state in which the first and second regions are of opposite conductivity type relative to one another.

8 Claims, 19 Drawing Sheets

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,049,970 A	9/1991	Tanaka et al.
5,122,476 A	6/1992	Fazan et al.
6,034,882 A	3/2000	Johnson et al.
6,218,696 B1	4/2001	Radius
6,432,767 B2	8/2002	Torli et al.
6,524,867 B2	2/2003	Yang et al.
6,552,952 B2	4/2003	Pascucci
6,687,147 B2	2/2004	Frickie et al.
6,693,821 B2	2/2004	Hsu et al.
6,693,846 B2	2/2004	Fibranz
6,717,881 B2	4/2004	Ooishi
6,753,561 B1	6/2004	Rinerson et al.
6,753,562 B1	6/2004	Hsu et al.
6,757,188 B2	6/2004	Perner et al.
6,778,421 B2	8/2004	Tran
6,785,159 B2	8/2004	Tuttle
6,806,531 B1	10/2004	Chen et al.
6,834,008 B2	12/2004	Rinerson et al.
6,873,544 B2	3/2005	Perner et al.
6,905,937 B2	6/2005	Hsu et al.
6,930,324 B2	8/2005	Kowalski et al.
6,940,113 B2	9/2005	Hsu et al.
6,946,702 B2	9/2005	Jang
6,950,369 B2	9/2005	Kunikiyo et al.
6,955,992 B2	10/2005	Zhang et al.
6,958,273 B2	10/2005	Chen et al.
6,961,258 B2	11/2005	Lowrey
6,970,375 B2	11/2005	Rinerson et al.
6,972,211 B2	12/2005	Hsu et al.
6,985,374 B2	1/2006	Yamamura
7,002,197 B2	2/2006	Perner et al.
7,005,350 B2	2/2006	Walker et al.
7,009,278 B2	3/2006	Hsu
7,026,911 B2	4/2006	Aono et al.
7,029,924 B2	4/2006	Hsu et al.
7,029,925 B2	4/2006	Celii et al.
7,035,141 B1	4/2006	Trispas et al.
7,046,550 B1	5/2006	Reohr et al.
7,050,316 B1	5/2006	Lin et al.
7,067,862 B2	6/2006	Rinerson et al.
7,085,167 B2	8/2006	Lee et al.
7,109,544 B2	9/2006	Schloesser et al.
7,123,535 B2	10/2006	Kurotsuchi et al.
7,149,108 B2	12/2006	Rinerson et al.
7,167,387 B2	1/2007	Sugita et al.
7,180,160 B2	2/2007	Ferrant et al.
7,187,201 B1	3/2007	Trimberger
7,193,267 B2	3/2007	Hsu et al.
7,205,238 B2	4/2007	Pan et al.
7,233,024 B2	6/2007	Scheuerlein et al.
7,236,389 B2	6/2007	Hsu
7,247,876 B2	7/2007	Lowrey
7,273,791 B2	9/2007	Basceri et al.
7,323,349 B2	1/2008	Hsu et al.
7,388,775 B2	6/2008	Bedeschi et al.
7,393,785 B2	7/2008	Uhlenbrock et al.
7,405,967 B2	7/2008	Kozicki et al.
7,459,715 B2	12/2008	Toda et al.
7,465,675 B2	12/2008	Koh
7,473,982 B2	1/2009	Aono et al.
7,489,552 B2	2/2009	Kurotsichi et al.
7,525,410 B2	4/2009	Aono et al.
7,538,338 B2	5/2009	Rinerson et al.
7,544,987 B2	6/2009	Lu et al.
7,557,424 B2	7/2009	Wong et al.
7,560,815 B1	7/2009	Vaartstra et al.
7,570,511 B2	8/2009	Cho et al.
7,639,523 B2	12/2009	Celinska et al.
7,666,526 B2	2/2010	Chen et al.
7,671,417 B2	3/2010	Yoshida et al.
7,679,812 B2	3/2010	Sasagawa et al.
7,687,793 B2	3/2010	Harshfield et al.
7,687,840 B2	3/2010	Shinmura
7,696,077 B2	4/2010	Liu
7,700,935 B2	4/2010	Kim et al.
7,727,908 B2	6/2010	Ahn et al.
7,751,163 B2	7/2010	Duch et al.
7,755,076 B2	7/2010	Lung
7,768,812 B2	8/2010	Liu
7,772,580 B2	8/2010	Hofmann et al.
7,777,215 B2	8/2010	Chien et al.
7,799,672 B2	9/2010	Hashimoto et al.
7,838,861 B2	11/2010	Klostermann
7,842,991 B2	11/2010	Cho et al.
7,864,568 B2	1/2011	Fujisaki et al.
7,898,839 B2	3/2011	Aoki
7,907,436 B2	3/2011	Maejima et al.
7,910,909 B2	3/2011	Kim et al.
7,948,784 B2	5/2011	Kajigaya
7,990,754 B2	8/2011	Azuma et al.
8,021,897 B2	9/2011	Sills et al.
8,043,926 B2	10/2011	Cho et al.
8,048,755 B2	11/2011	Sandhu et al.
8,094,477 B2	1/2012	Maejima
8,098,520 B2	1/2012	Seigler et al.
8,106,375 B2	1/2012	Chen et al.
8,114,468 B2	2/2012	Sandhu et al.
8,124,968 B2	2/2012	Koo et al.
8,154,908 B2	4/2012	Maejima et al.
8,154,909 B2	4/2012	Azuma et al.
8,295,077 B2	10/2012	Murooka
8,355,274 B2	1/2013	Arita et al.
8,411,477 B2	4/2013	Tang et al.
8,427,859 B2	4/2013	Sandhu et al.
8,431,458 B2	4/2013	Sills et al.
8,436,414 B2	5/2013	Tanaka et al.
8,536,556 B2	9/2013	Fukumizu
8,537,592 B2	9/2013	Liu
8,542,513 B2	9/2013	Tang et al.
8,611,121 B2	12/2013	Ahn et al.
8,652,909 B2	2/2014	Sills et al.
8,743,589 B2	6/2014	Sandhu et al.
8,791,447 B2	7/2014	Liu et al.
8,854,863 B2	10/2014	Liu
2002/0018355 A1	2/2002	Johnson et al.
2002/0034117 A1	3/2002	Okazawa
2002/0079524 A1	6/2002	Dennison
2002/0196695 A1	12/2002	Pascucci
2003/0031047 A1	2/2003	Anthony et al.
2003/0086313 A1	5/2003	Asao
2003/0174042 A1	9/2003	Aono et al.
2003/0174570 A1	9/2003	Oishi
2003/0185049 A1	10/2003	Fricke et al.
2003/0218902 A1	11/2003	Perner et al.
2003/0218929 A1	11/2003	Fibranz
2003/0223283 A1	12/2003	Kunikiyo
2004/0002186 A1	1/2004	Vyvoda et al.
2004/0090841 A1	5/2004	Perner et al.
2004/0100835 A1	5/2004	Sugibayashi et al.
2004/0108528 A1	6/2004	Hsu et al.
2004/0124407 A1	7/2004	Kozicki et al.
2004/0188714 A1	9/2004	Scheuerlein
2004/0245547 A1	12/2004	Stipe
2005/0001257 A1	1/2005	Schoelesser et al.
2005/0014325 A1	1/2005	Aono et al.
2005/0032100 A1	2/2005	Heath et al.
2005/0054119 A1	3/2005	Hsu et al.
2005/0128799 A1	6/2005	Kurotsuchi et al.
2005/0161747 A1	7/2005	Lung et al.
2005/0174835 A1	8/2005	Rinerson et al.
2005/0205943 A1	9/2005	Yamada
2005/0243844 A1	11/2005	Aono et al.
2005/0250281 A1	11/2005	Ufert et al.
2005/0269646 A1	12/2005	Yamada
2005/0275003 A1	12/2005	Shinmura
2005/0287741 A1	12/2005	Ding
2006/0035451 A1	2/2006	Hsu
2006/0046509 A1	3/2006	Gwan-Hyeob
2006/0062049 A1	3/2006	Lee et al.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2006/0097238 A1	5/2006	Breuil et al.
2006/0099813 A1	5/2006	Pan et al.
2006/0104111 A1	5/2006	Tripsas et al.
2006/0110878 A1	5/2006	Lung et al.
2006/0160304 A1	7/2006	Hsu et al.
2006/0170027 A1	8/2006	Lee et al.
2006/0171200 A1	8/2006	Rinerson et al.
2006/0181920 A1	8/2006	Ufert
2006/0215445 A1*	9/2006	Baek et al. 365/158
2006/0258079 A1	11/2006	Lung et al.
2006/0258089 A1	11/2006	Chung-Zen
2006/0274593 A1	12/2006	Kurotsuchi et al.
2006/0284242 A1	12/2006	Jo
2006/0286709 A1	12/2006	Lung et al.
2007/0010082 A1	1/2007	Pinnow et al.
2007/0015330 A1	1/2007	Li et al.
2007/0019923 A1	1/2007	Sasagawa et al.
2007/0034848 A1	2/2007	Liu
2007/0041235 A1	2/2007	Inoue
2007/0045615 A1	3/2007	Cho et al.
2007/0048990 A1	3/2007	Zhuang et al.
2007/0086235 A1	4/2007	Kim et al.
2007/0109835 A1	5/2007	Hsu
2007/0120124 A1	5/2007	Chen et al.
2007/0121369 A1	5/2007	Happ
2007/0123039 A1	5/2007	Elkins et al.
2007/0132049 A1	6/2007	Stipe
2007/0165434 A1	7/2007	Lee et al.
2007/0167008 A1	7/2007	Hsu et al.
2007/0171706 A1	7/2007	Fuji
2007/0173019 A1	7/2007	Ho et al.
2007/0176261 A1	8/2007	Lung
2007/0210348 A1	9/2007	Song et al.
2007/0224770 A1	9/2007	Nagashima
2007/0231988 A1	10/2007	Yoo et al.
2007/0246795 A1	10/2007	Fang et al.
2007/0257257 A1	11/2007	Cho et al.
2007/0258279 A1	11/2007	Lung et al.
2007/0267675 A1	11/2007	Cho et al.
2007/0268739 A1	11/2007	Yoo et al.
2007/0268742 A1	11/2007	Liu
2007/0269683 A1	11/2007	Chen et al.
2007/0278578 A1	12/2007	Yoshida et al.
2007/0285965 A1	12/2007	Toda et al.
2007/0295950 A1	12/2007	Cho et al.
2008/0001172 A1	1/2008	Karg et al.
2008/0008642 A1	1/2008	Mori et al.
2008/0012064 A1	1/2008	Park et al.
2008/0013363 A1	1/2008	Kim et al.
2008/0014750 A1	1/2008	Nagashima
2008/0026547 A1	1/2008	Yin et al.
2008/0029754 A1	2/2008	Min et al.
2008/0029842 A1	2/2008	Symanczyk
2008/0036508 A1	2/2008	Sakamoto et al.
2008/0048165 A1	2/2008	Miyazawa
2008/0049487 A1	2/2008	Yoshimura et al.
2008/0062740 A1	3/2008	Baek et al.
2008/0073635 A1	3/2008	Kiyotoshi et al.
2008/0078985 A1	4/2008	Meyer et al.
2008/0080229 A1	4/2008	Choi et al.
2008/0089105 A1	4/2008	Ro et al.
2008/0093591 A1	4/2008	Khang et al.
2008/0099753 A1	5/2008	Song et al.
2008/0102278 A1	5/2008	Kreupl et al.
2008/0105862 A1	5/2008	Lung et al.
2008/0106925 A1*	5/2008	Paz de Araujo et al. 365/148
2008/0123390 A1	5/2008	Kim et al.
2008/0157257 A1	7/2008	Bertin et al.
2008/0175031 A1	7/2008	Park et al.
2008/0175032 A1	7/2008	Tanaka et al.
2008/0185571 A1	8/2008	Happ et al.
2008/0185687 A1	8/2008	Hong et al.
2008/0212361 A1	9/2008	Bertin et al.
2008/0232160 A1	9/2008	Gopalakrishnan
2008/0247219 A1	10/2008	Choi et al.
2008/0251779 A1	10/2008	Kakosehke et al.
2008/0258126 A1	10/2008	Lung
2008/0259672 A1	10/2008	Lung
2008/0303014 A1	12/2008	Goux et al.
2009/0014706 A1	1/2009	Lung
2009/0014707 A1	1/2009	Lu et al.
2009/0026436 A1	1/2009	Song et al.
2009/0057640 A1	3/2009	Lin et al.
2009/0059644 A1	3/2009	Kajigaya et al.
2009/0072217 A1	3/2009	Klostermann
2009/0085121 A1	4/2009	Park et al.
2009/0097295 A1	4/2009	Morimoto
2009/0141547 A1	6/2009	Jin et al.
2009/0168495 A1	7/2009	Aoki
2009/0173930 A1	7/2009	Yasuda et al.
2009/0180309 A1	7/2009	Liu
2009/0207647 A1	8/2009	Maejima et al.
2009/0207681 A1	8/2009	Juengling
2009/0218557 A1	9/2009	Sato
2009/0250681 A1	10/2009	Smythe et al.
2009/0261314 A1	10/2009	Kim et al.
2009/0261343 A1	10/2009	Herner et al.
2009/0267047 A1	10/2009	Sasago et al.
2009/0268532 A1	10/2009	DeAmbroggi et al.
2009/0272959 A1*	11/2009	Phatak et al. 257/2
2009/0272960 A1	11/2009	Srinivasan et al.
2009/0272961 A1*	11/2009	Miller et al. 257/4
2009/0272962 A1*	11/2009	Kumar et al. 257/4
2009/0273087 A1*	11/2009	French et al. 257/761
2009/0278109 A1*	11/2009	Phatak 257/4
2009/0303780 A1	12/2009	Kasko et al.
2009/0315090 A1	12/2009	Weis et al.
2009/0316467 A1	12/2009	Liu
2009/0316474 A1	12/2009	Cho et al.
2009/0317540 A1	12/2009	Sandhu et al.
2009/0321878 A1	12/2009	Koo et al.
2009/0323385 A1	12/2009	Scheurelein et al.
2010/0003782 A1	1/2010	Sinha et al.
2010/0008163 A1	1/2010	Liu
2010/0044666 A1*	2/2010	Baek et al. 257/2
2010/0046273 A1	2/2010	Azuma et al.
2010/0061132 A1	3/2010	Fujisaki et al.
2010/0065836 A1	3/2010	Lee et al.
2010/0072452 A1	3/2010	Kim et al.
2010/0084741 A1	4/2010	Andres et al.
2010/0085798 A1	4/2010	Lu et al.
2010/0090187 A1	4/2010	Ahn et al.
2010/0110759 A1	5/2010	Jin et al.
2010/0123542 A1	5/2010	Vaithyanathan et al.
2010/0135061 A1	6/2010	Li et al.
2010/0140578 A1	6/2010	Tian et al.
2010/0157657 A1	6/2010	Rinerson et al.
2010/0157658 A1	6/2010	Schloss et al.
2010/0163820 A1	7/2010	Son
2010/0163829 A1	7/2010	Wang et al.
2010/0172171 A1	7/2010	Azuma et al.
2010/0176368 A1	7/2010	Ko et al.
2010/0178729 A1	7/2010	Yoon et al.
2010/0193758 A1	8/2010	Tian et al.
2010/0193761 A1	8/2010	Amin et al.
2010/0193762 A1	8/2010	Hsieh et al.
2010/0195371 A1	8/2010	Ohba et al.
2010/0232200 A1	9/2010	Shepard
2010/0237442 A1	9/2010	Li et al.
2010/0243983 A1*	9/2010	Chiang et al. 257/4
2010/0258782 A1*	10/2010	Kuse et al. 257/4
2010/0259960 A1	10/2010	Samachisa
2010/0259961 A1	10/2010	Fasoli et al.
2010/0259962 A1	10/2010	Yan et al.
2011/0059576 A1	3/2011	Cho et al.
2011/0128775 A1	6/2011	Maejima et al.
2011/0171836 A1	7/2011	Xia
2011/0193044 A1	8/2011	Sandhu et al.
2011/0205783 A1	8/2011	Murooka
2011/0249486 A1	10/2011	Azuma et al.
2011/0261606 A1	10/2011	Sandhu et al.
2011/0261607 A1	10/2011	Tang et al.
2011/0309322 A1	12/2011	Hwang
2012/0119180 A1	5/2012	Koo et al.

(56)   References Cited

U.S. PATENT DOCUMENTS

2012/0140542 A1   6/2012   Liu
2012/0147648 A1   6/2012   Scheuerlein
2012/0164798 A1   6/2012   Sills et al.
2012/0187363 A1   7/2012   Liu et al.
2012/0248399 A1   10/2012   Sasago et al.
2013/0021836 A1   1/2013   Liu
2014/0247640 A1   9/2014   Liu

FOREIGN PATENT DOCUMENTS

CN   1459792   12/2003
CN   1624803   6/2005
CN   101005113   12/2006
CN   101051670   4/2007
CN   101034732   9/2007
CN   101256831   9/2008
CN   101350360   1/2009
CN   101546602   9/2009
CN   101840995   9/2010
CN   200880124714   7/2012
CN   201180027954   5/2014
CN   201180065042   5/2015
CN   2011800578660   11/2015
EP   GB 1266513   3/1972
EP   1796103   9/2006
EP   11796103   9/2006
EP   11792836   12/2013
EP   11845727.4   11/2014
EP   11834802   3/2015
EP   14171745   3/2015
JP   2005175457   6/2005
JP   2005-353779   12/2005
JP   2006032729   2/2006
JP   2006040981   2/2006
JP   2006074028   3/2006
JP   2006121044   5/2006
JP   2008-135744   6/2008
JP   2008-192995   8/2008
JP   2009-081251   4/2009
JP   2009-163867   7/2009
JP   2009-267411   11/2009
JP   2010-009669   1/2010
JP   2010-010688   1/2010
JP   2010-192569   9/2010
JP   2010-192646   9/2010
JP   2010-232214   10/2010
JP   2010-263211   11/2010
KR   2003-0048421   6/2003
KR   2005-0008353   1/2005
KR   1020060087882   8/2006
KR   10-0751736   8/2007
KR   20070111840   11/2007
KR   20070118865   12/2007
KR   20090109804   10/2009
KR   20100078808   7/2010
KR   20100083402   7/2010
TW   097147549   5/2013
TW   100119681   8/2013
TW   100142963   8/2014
TW   101102280   8/2014
WO   WO 2006/003620   1/2006
WO   WO 2008/029446   3/2008
WO   PCT/US2008/084422   3/2009
WO   WO 2009/127187   10/2009
WO   WO 2010/068221   6/2010
WO   2010/082922   7/2010
WO   WO 2010/082923   7/2010
WO   WO 2010/082928   7/2010
WO   WO 2010/085241   7/2010
WO   WO 2010/087854   8/2010
WO   WO 2010/101340   9/2010
WO   WO 2010/117911   10/2010
WO   PCT/US2011/035601   11/2011
WO   PCT/US2011/051785   4/2012
WO   PCT/US2011/059095   5/2012
WO   PCT/US12/021168   7/2012
WO   PCT/US2011/066770   9/2012
WO   PCT/US11/035601   12/2012
WO   WO   8/2013
       PCT/US2012/021168

OTHER PUBLICATIONS

U.S. Appl. No. 12/765,598, filed Apr. 22, 2010, Sandhu et al.
U.S. Appl. No. 12/959,015, filed Dec. 2, 2010, Liu.
U.S. Appl. No. 12/979,189, filed Dec. 27, 2010, Sills et al.
U.S. Appl. No. 13/010,048, filed Jan. 20, 2011, Liu et al.
U.S. Appl. No. 12/014,232, filed Jan. 15, 2008, Liu.
U.S. Appl. No. 12/099,267, filed Apr. 8, 2008, Smythe et al.
U.S. Appl. No. 12/114,096, filed May 2, 2008, Srinivasan et al.
U.S. Appl. No. 12/141,388, filed Jun. 18, 2008, Liu et al.
U.S. Appl. No. 12/141,559, filed Jun. 18, 2008, Sandhu et al.
U.S. Appl. No. 12/166,604, filed Jul. 2, 2008, Sinha et al.
U.S. Appl. No. 12/765,606, filed Apr. 22, 2010, Tang et al.
Baek et al., "Multi-Layer cross-point Binary Oxide resistive Memory (OxRRAM) for Post-NAND Storage Application", IEEE, 2005.
Bedeschi et al., "A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage", IEEE, vol. 44, No. 1, Jan. 2009, pp. 217-227.
Chen et al., "Non-Volatile Resistive Switching for Advanced Memory Applications", IEEE, 2005, 4 pages.
Chen et al., Peroskite RRAM Devices with Metal/Insulator/PCMO/Metal Heterostructures, 2005; pp. 125-128.
Choi et al., "Defect Structure and Electrical Properties of single-Crystal Ba0.03SR0.97TiO3", J. Am Ceram. Soc., 71, [4], pp. 201-205, 1988.
Courtade et al., "Microsturcture and resistance switching in NiO binary oxide films obtained from Ni oxidation", IEEE, 2006, pp. 94-99.
Higaki et al., "Effects of Gas Phase Absorption into Si Substrates on Plasma doping Process" A208.
Ho et al., "A Highly Reliable Self-=Aligned Graded Oxide WOx Resistance Memory: Conduction Mechanisms and Reliability", 2007 Symposium on VLSI Technology Digest of Technical Papers, pp. 228-229.
Hosoi et al., "High Speed Unipolar Switching Resistance RAM (RRAM) Technology", Advanced Materials Res. Lab, Japan; Correlated Electron Res. Center (CERC), Japan; Nanotechnology Res. Inst. (NRI), Japan, Dec. 2006; 4 pp.
Hudgens et al., "Overview of Phase-Change Chalcogenide Nonvolatile Memory Technology", MRS Bulletin, Nov. 2004, pp. 829-832.
Ignatiev et al., "Resistance Non-volatile Memory-RRAM", Mater. Res. Soc. Symp. Proc., vol. 997, 2007, Materials Research Society, 9 pages.
Karg et al., "Nanoscale REsistive Memory Device using SrRiO3 Films", IEEE, 2007, pp. 68-70.
Kau et al., "A Stackable cross point phase change memory", IEEE, 2009, pp. 27.1.1-27.1.4.
Komori et al., Disturbless flash memory due to high boost efficiency on BiCS structure and optimal memory film stack for ultra high density storage device; Dec. 2008; pp. 851-854.
Kooij et al., "Photoselective Metal Deposition on Amorphous Silicon p-i-n Solar Cells", Electrochemical Society Letters, Journal of Electrochemical Society vol. 44, No. 10, Oct. 1997, pp. L271-L272.
Kozicki et al., "Non-Volatile Memory Based on Solid Electrolytes", Center for Solid States Electronics Research, Arizona State Univeristy, Nov. 2004; 8 pp.
Kozicki, "Memory Devices Based on Solid Electrolytes", Mater. Res. Soc. Symp. Proc., vol. 997, 2007, Materials Research Society, 10 pages.
Lee et al., "2-stack 1D-1R Cross-Point with Oxide Diodes as Switch Elements for High Density Resistance RAM Applications", IEEE, 2007, pp. 771-774.
Lee et al., "Resistance Switching of Al doped ZnO for Non-Volatile Memory Applications", Dept. of Materials Science and Engineering, Gwangju Institute of Science and Technology, 2 pages.

(56)   **References Cited**

OTHER PUBLICATIONS

Lin et al., "Effect of Top Electrode Material on Resistive Switching Properties of ZrO2 Film Memory Devices", IEEE, May 2007, vol. 28, No. 5, pp. 366-368.

Meyer et al., "Oxide Dual-Layer Memory Element for Scalable Non-Volatile Cross-Point Memory Technology", IEEE, 2008, 5 pages.

Miyashita et al., "A Novel Bit-Line Process using Poly-Si Masked Dual-Damascene (PMDD) for 0.13 um DRAMs and Beyond", IEEE, 2000, pp. 15.4.1-15.4.4.

Muller et al., "Emerging Non-Volatile Memory Technologies", IEEE, 2003, pp. 37-44.

Oh, "Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology" 2006, IEEE, 4 pages.

Pein et al., "Performance of the 3-D Pencil Flash EPROM Cell and Memory Array", IEEE, 1995, pp. 1982-1991.

Pellizzer et al., "A 90nm Phase Change Memory Technology for Stand-Alone Non-Volatile Memory Applications", IEEE, 2006, Symposium on VLSI Technology Digest of Technical Papers, 2 pages.

Pirovano et al., "Self-Aligned u Trench Phase-Change Memory Cell Architecture for 90nm Technology and Beyond", IEEE, 2007, pp. 222-225.

Programmable metallization cell, Dec. 11, 2007; http://en.wikipedia.org/wiki/Programmable_metallization_cell on Dec. 13, 2011.

Scheck et al., "Selective Metal Electrodeposition Through Doping Modulation of Semiconductor Surfaces". Applied Physics Letters 86, 2005, 3 pgs.

Website, http://en.wikipedia.org/wiki/Programmable_metalliza-tion_cell, 4 pages.

Wuttig, "Towards a Universal Memory?", Nature Materials, vol. 4, Apr. 2005, pp. 265-266.

Xing et al., "Characterization of AlGaN/GaN p-n Diodes with Selectively Regrown n-AlGaN by Metal-Organic Chemical-Vapor Deposition and its Application to GaN-Based Bipolar Transistors", Journal of Allpied Physics 97, 2005, 4 pgs.

Yih et al., "SiC/Si Heterojunction Diodes Fabricated by Self-Selective and by Blanket Rapid Thermal Chemical Vapor Deposition", IEEE vol. 41 No. 3, Mar. 1994, pp. 281-287.

Yoon et al., "Vertical Cross-Point Resistance Change Memory for Ultra-High Density Non-volatile Memory Applications", 2009 Symposium on VLSI Technology Digest of Technical Papers, pp. 26-27.

Yu et al., "Structure Effects on Resistive Switching of Al/TiOx/Al Devices for RRAM Applications", IEEE, 2008, pp. 331-333.

* cited by examiner
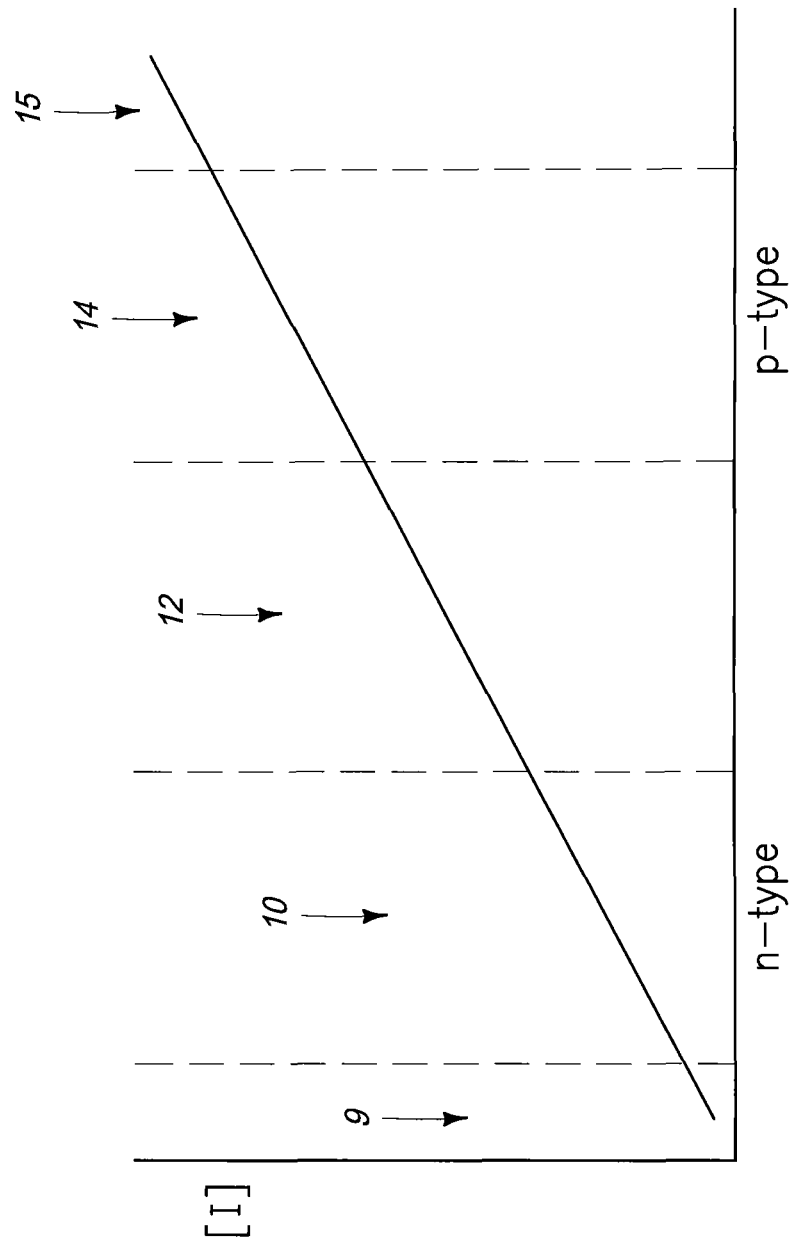
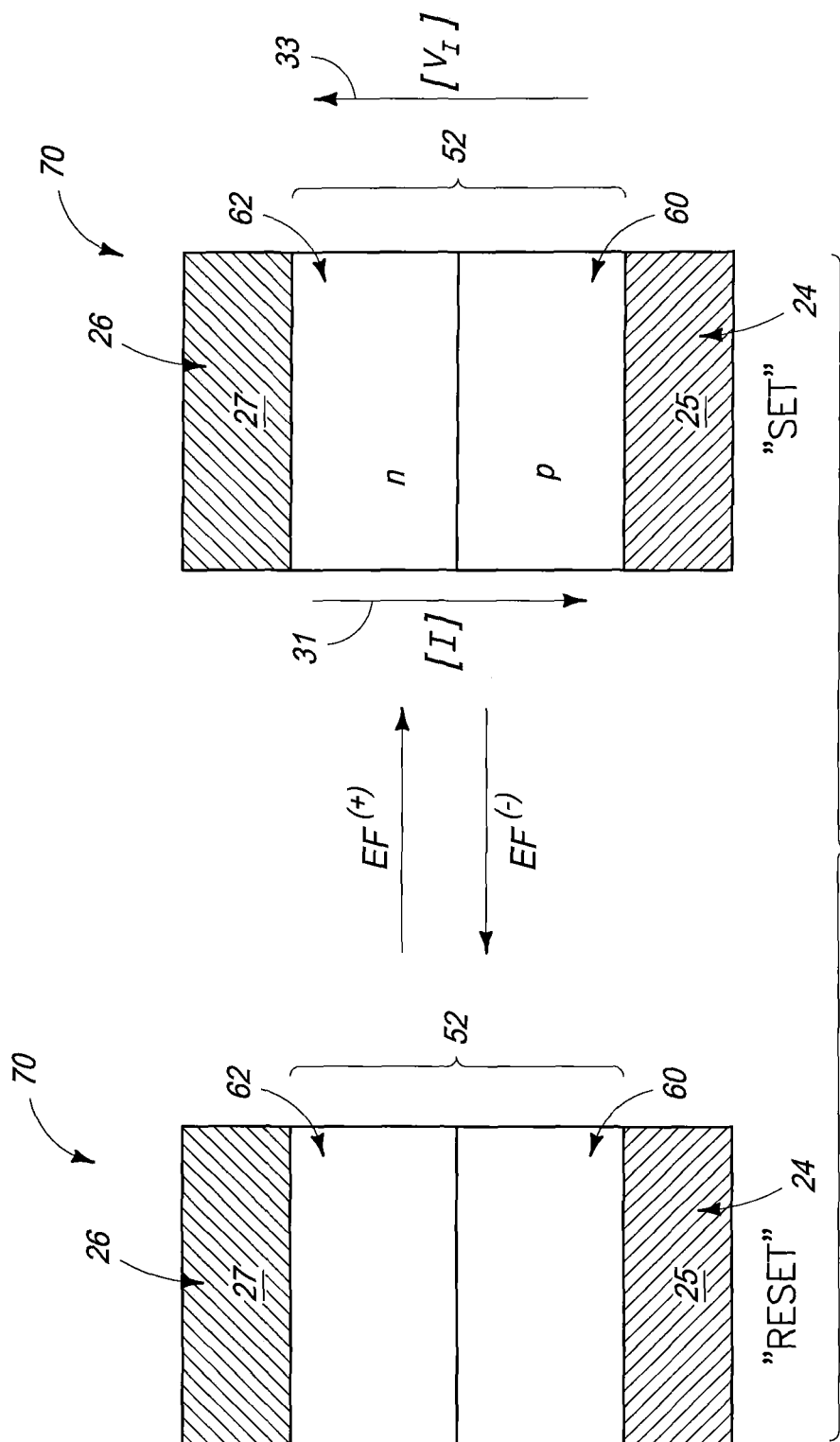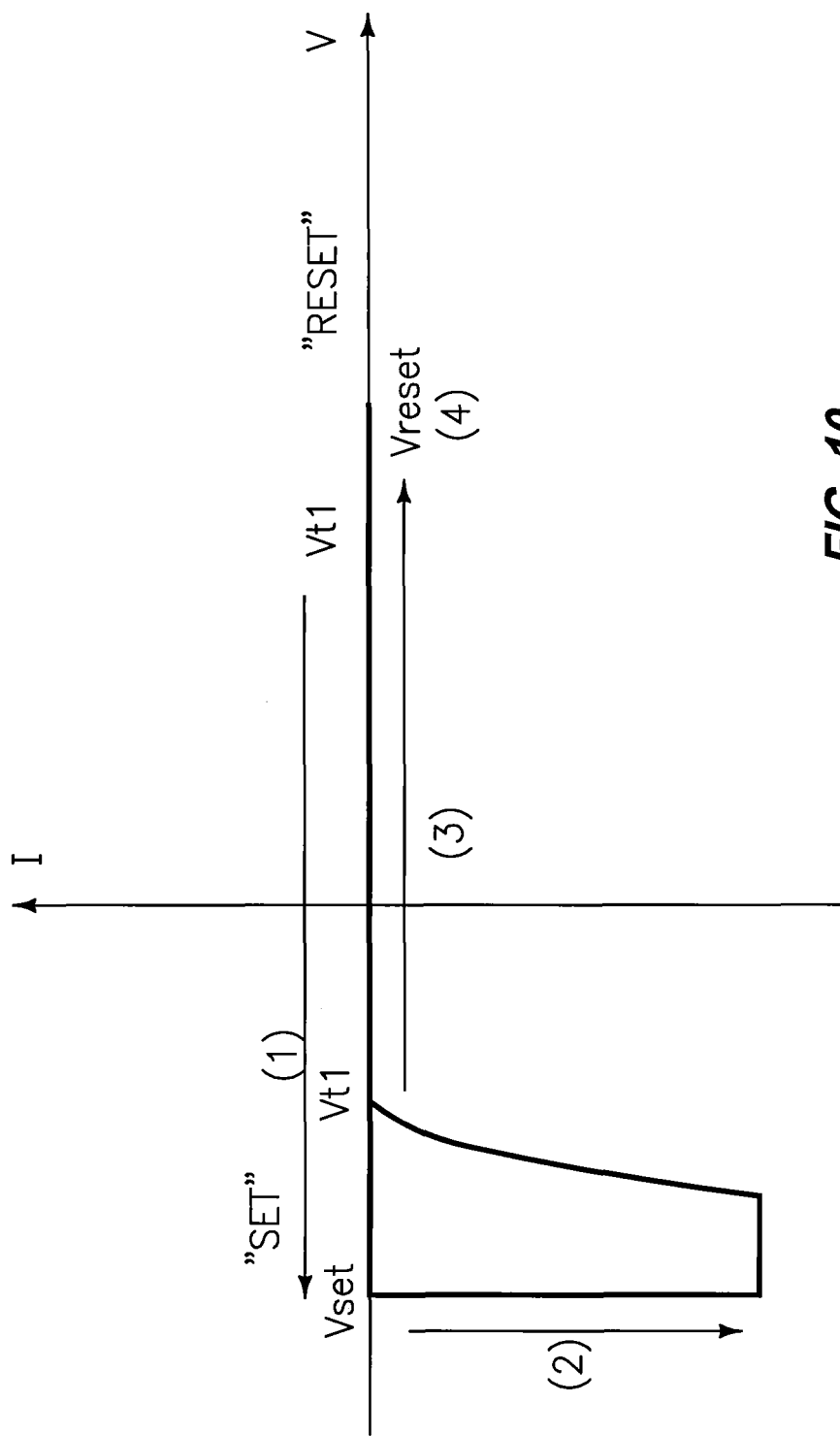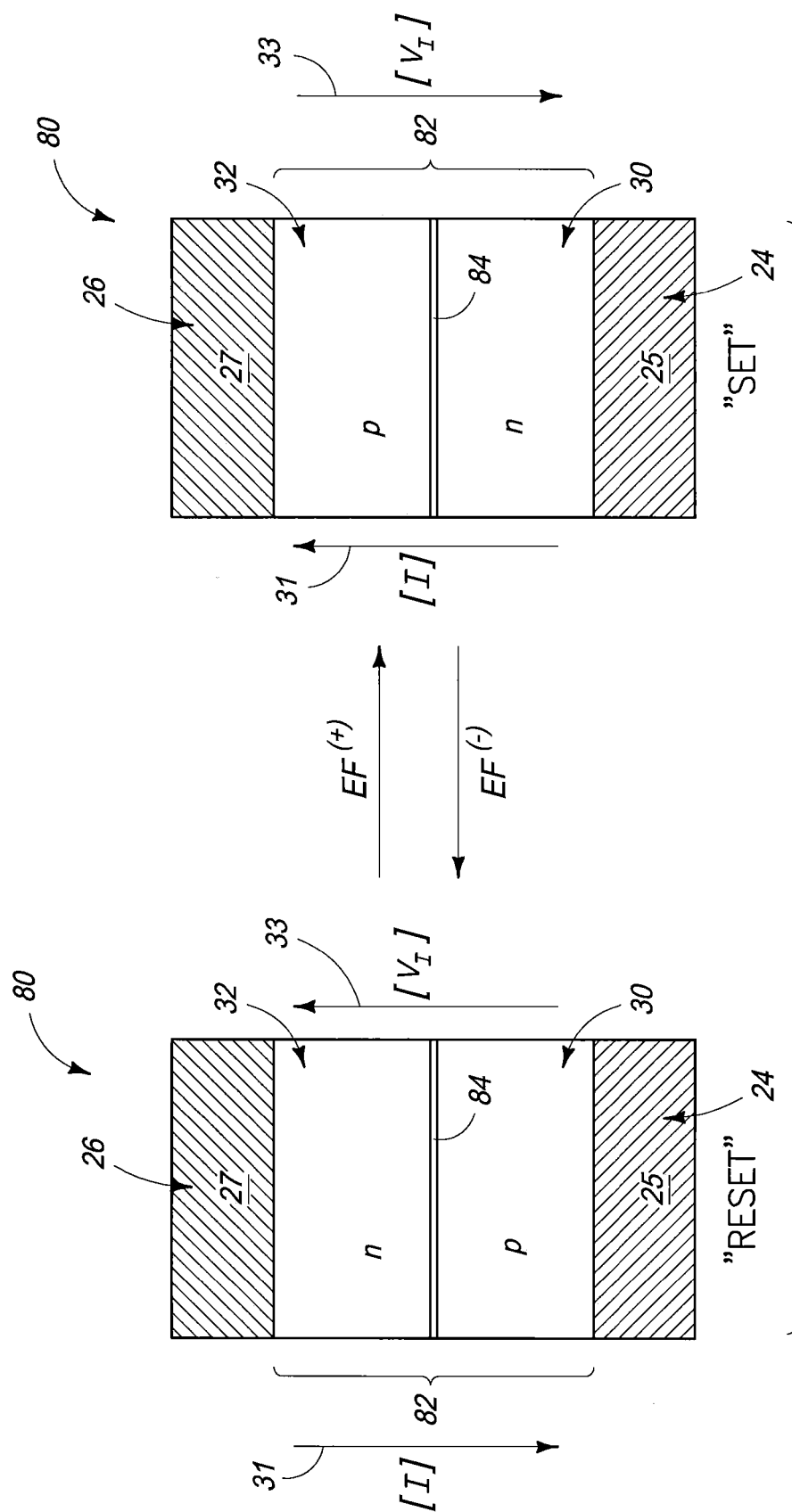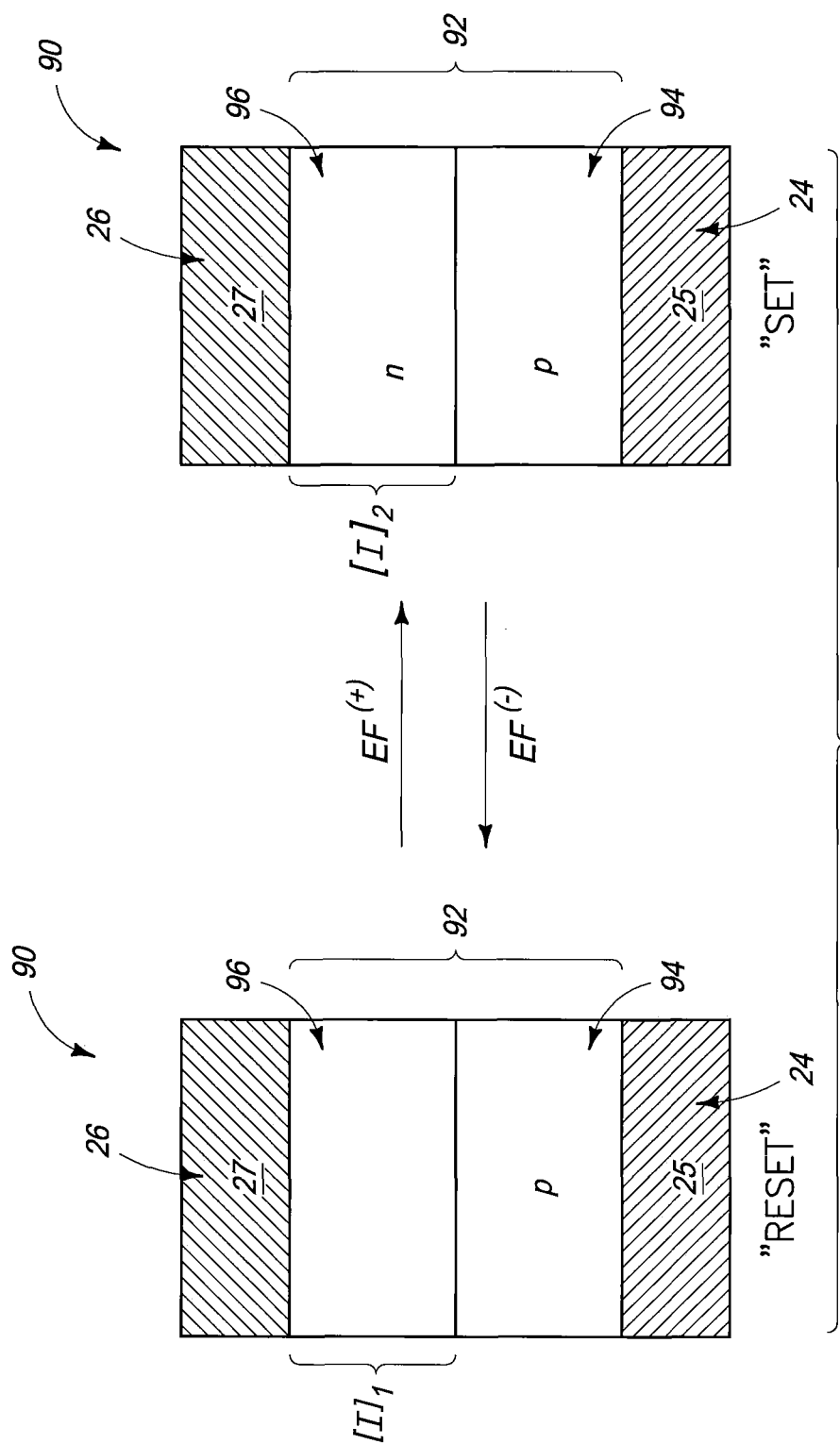*FIG. 1*

FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG. 6

FIG. 7
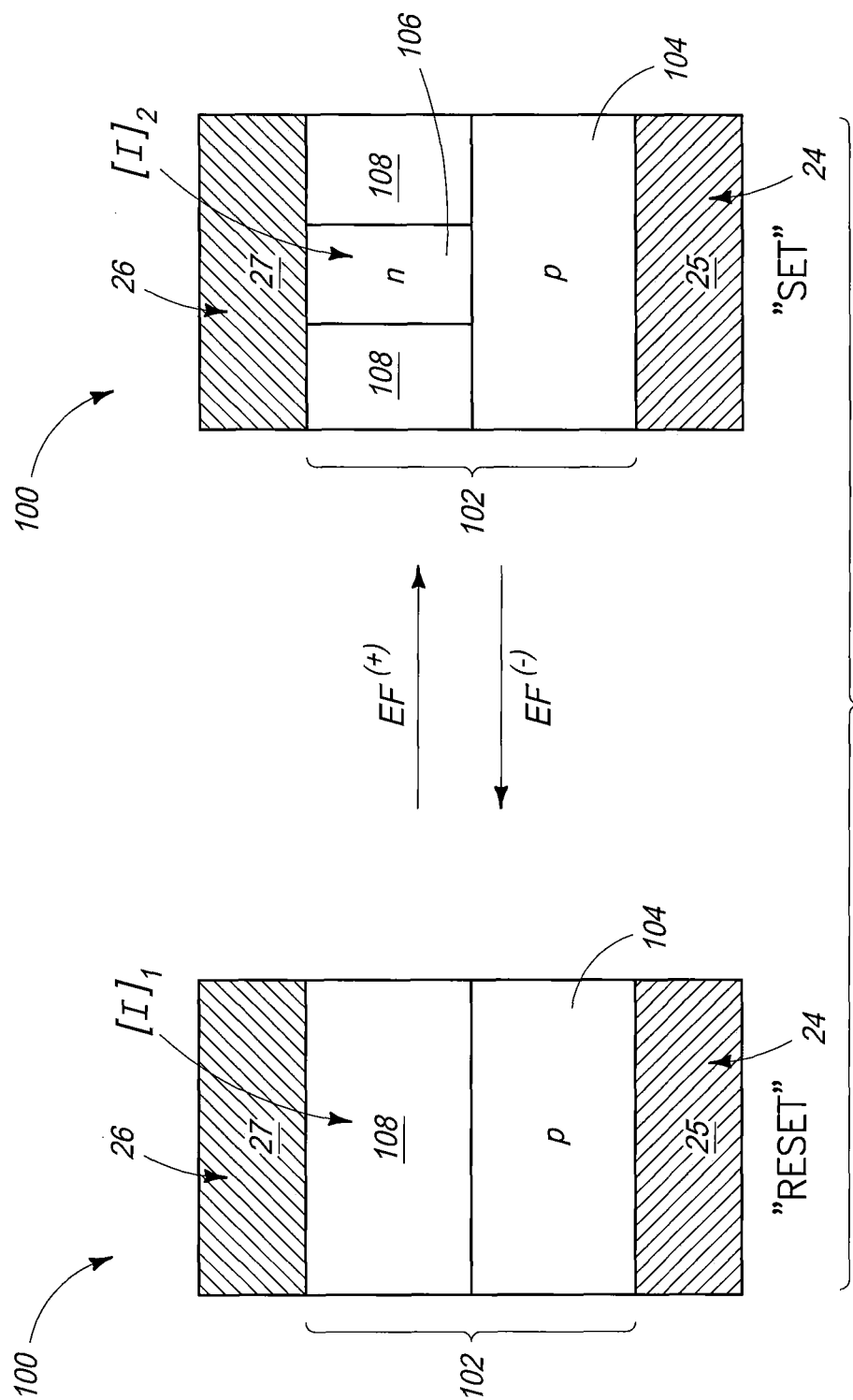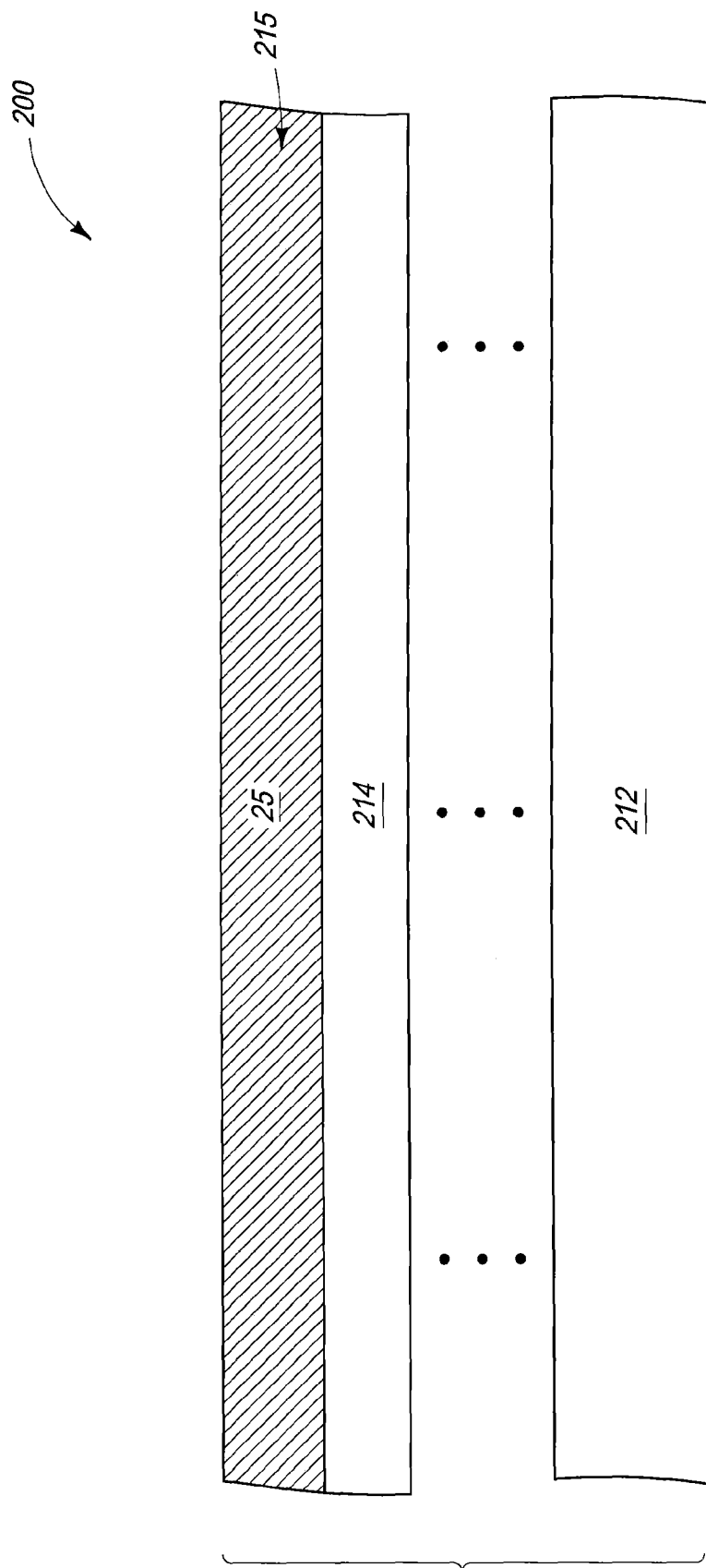
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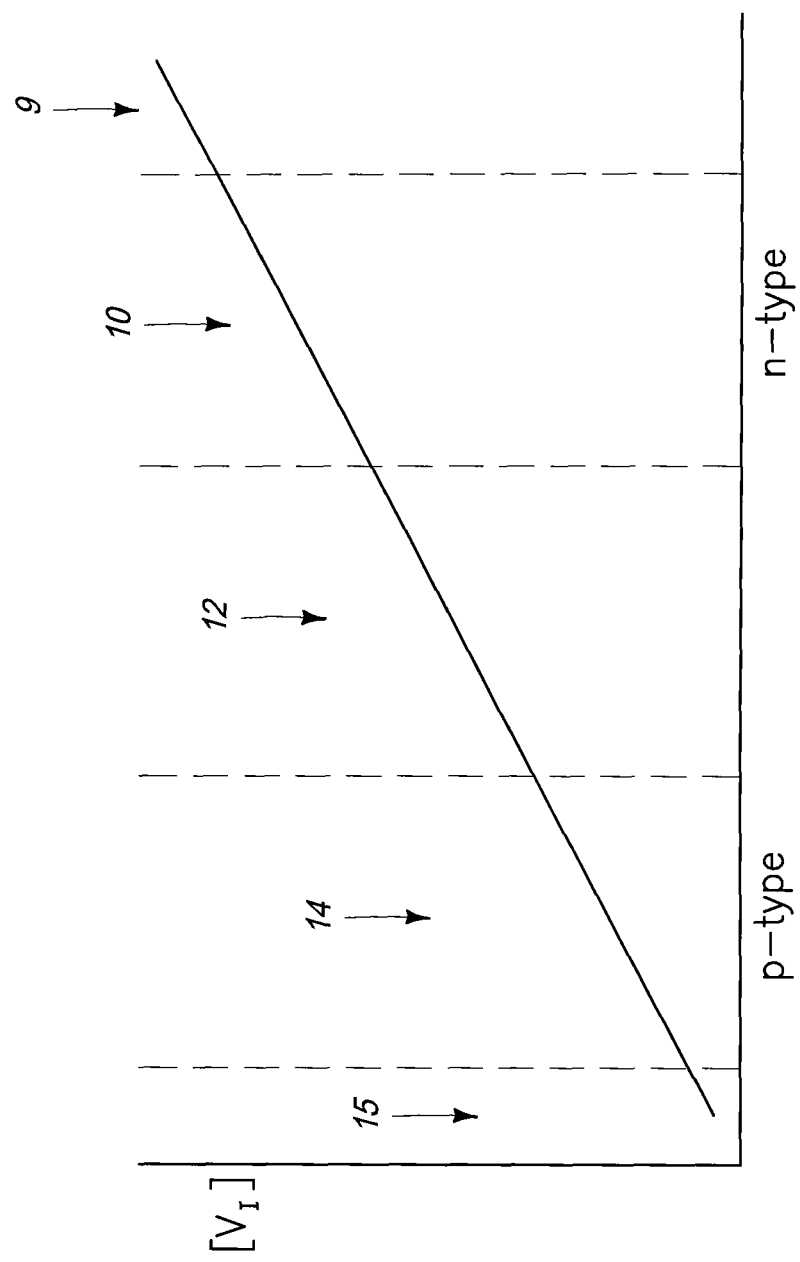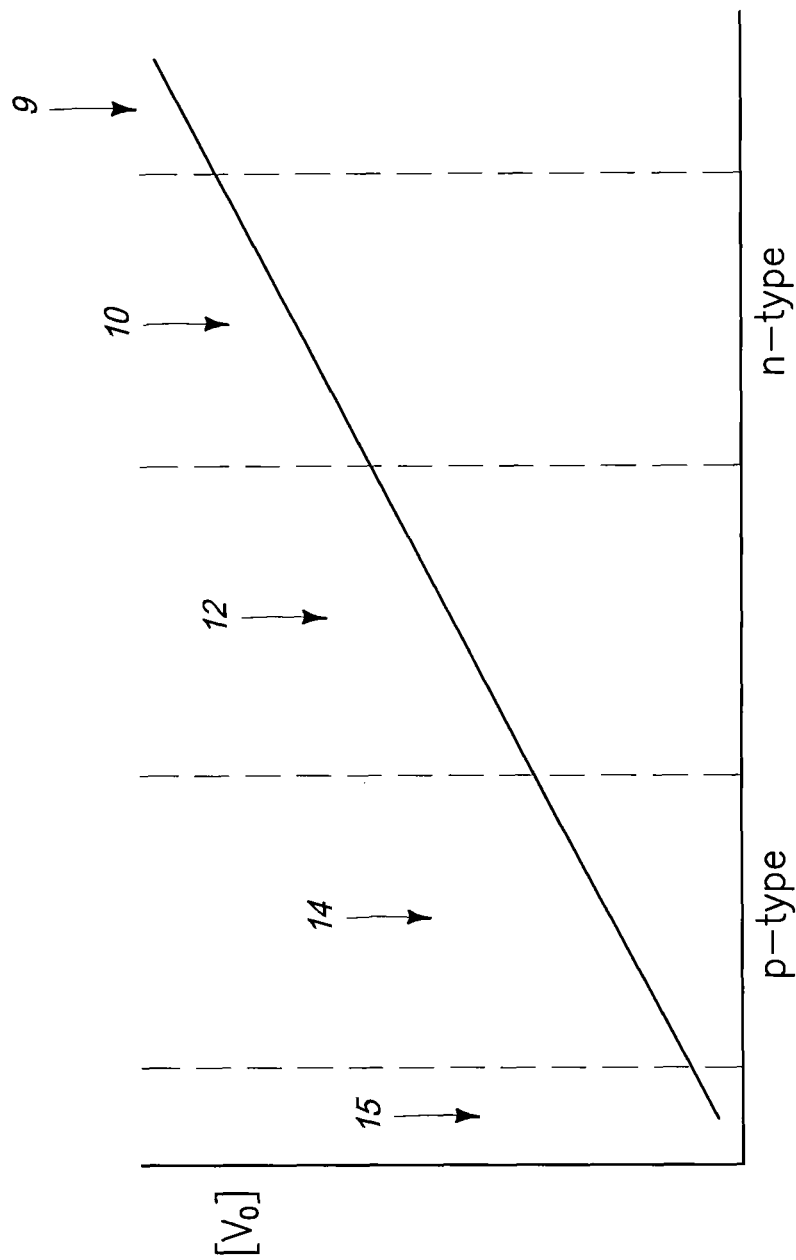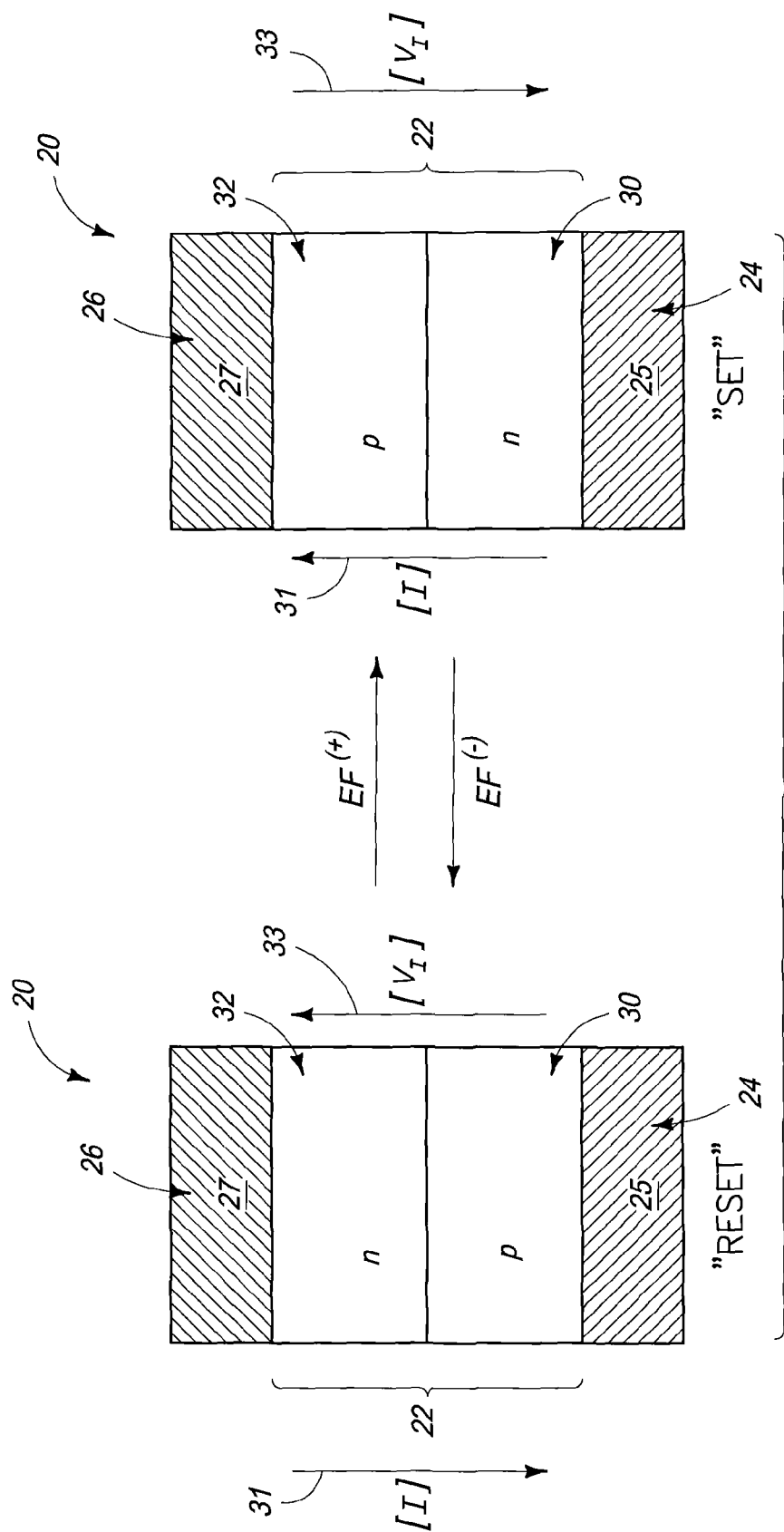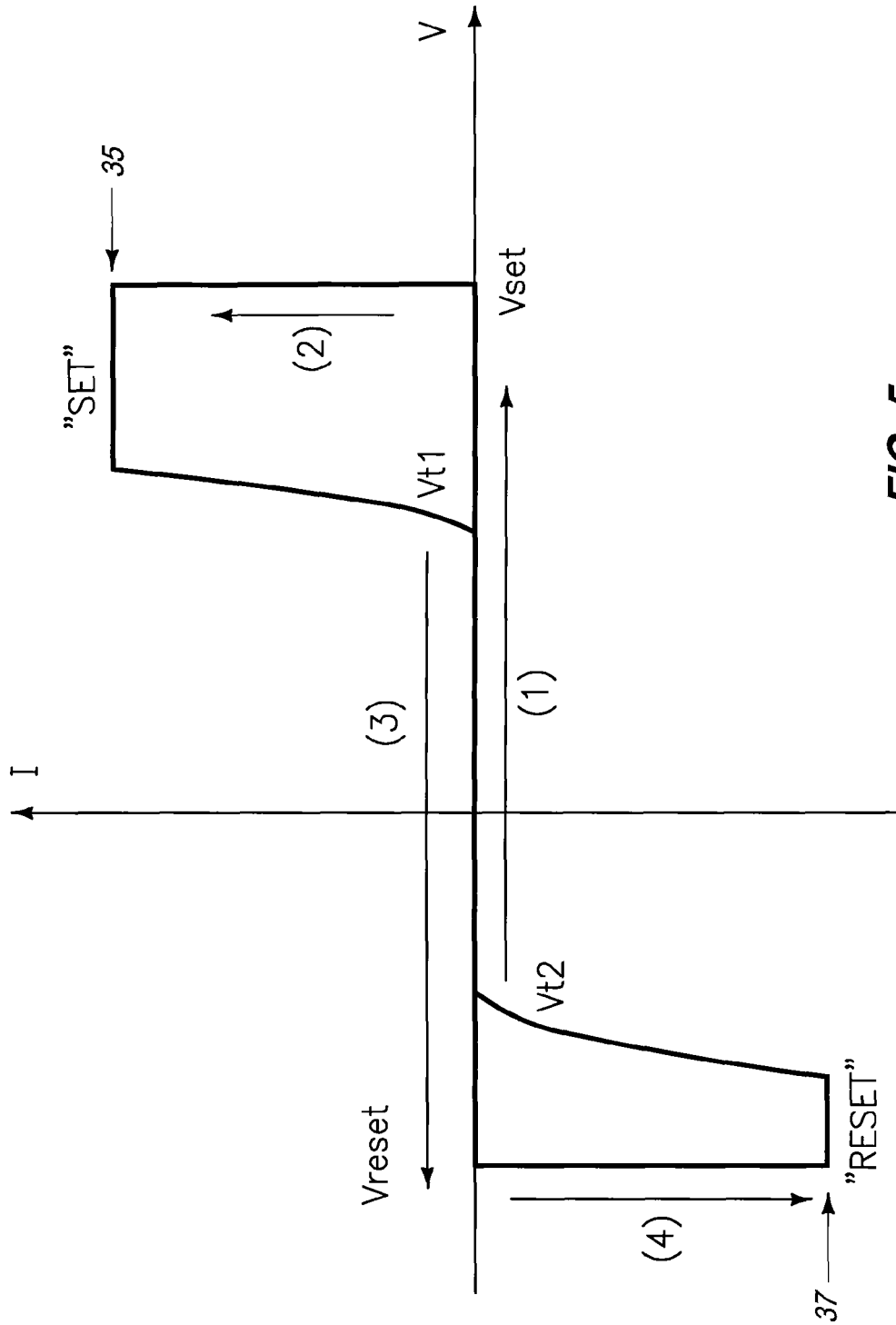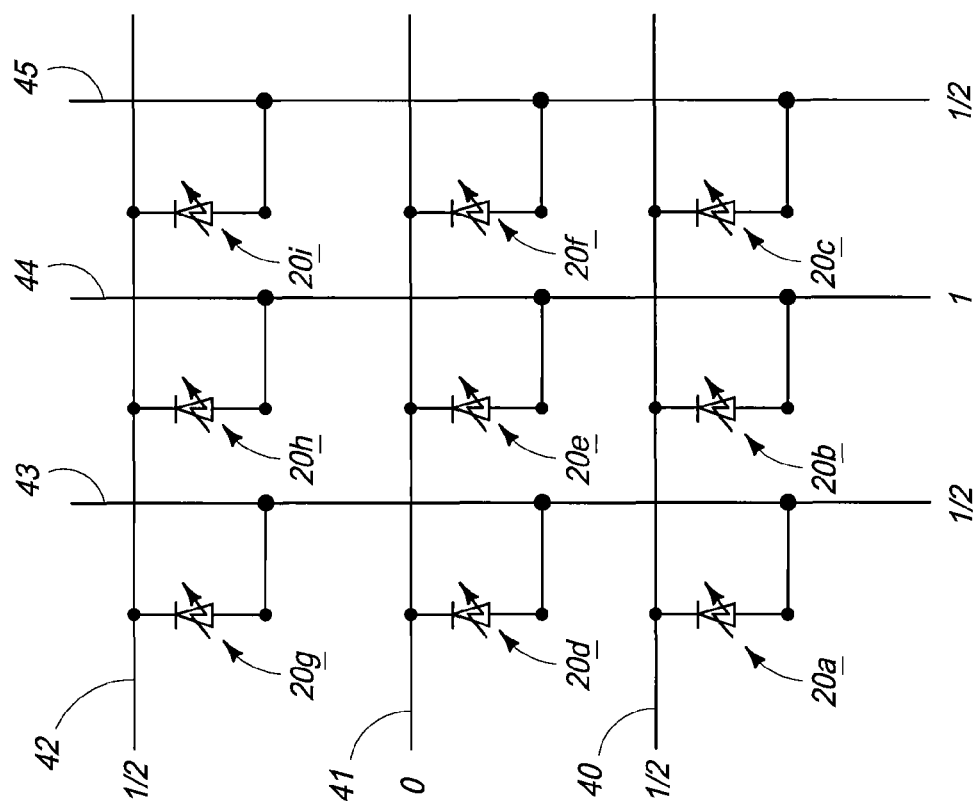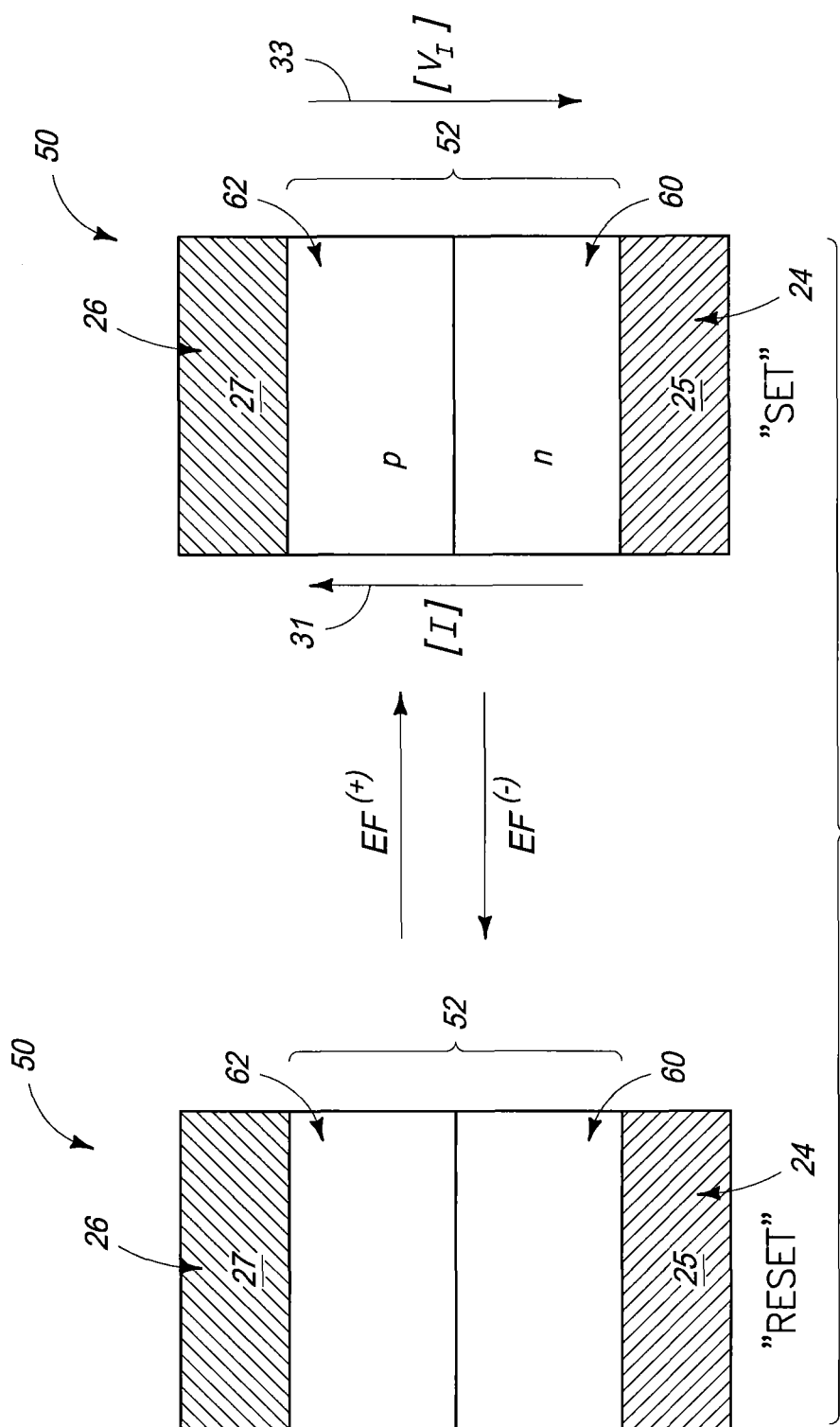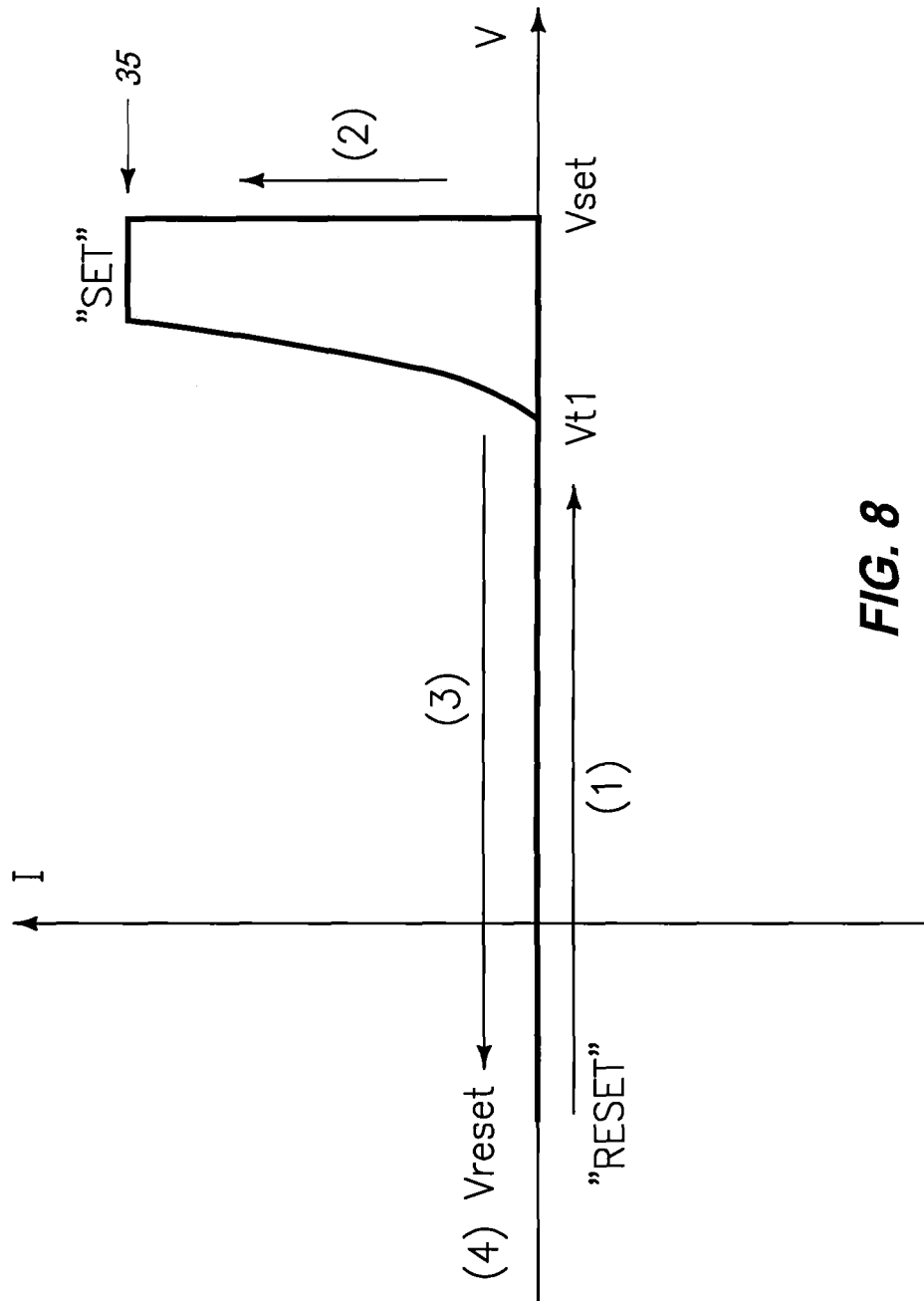
FIG. 9

FIG. 10

FIG. 11

FIG. 12

FIG. 13

FIG. 14

200

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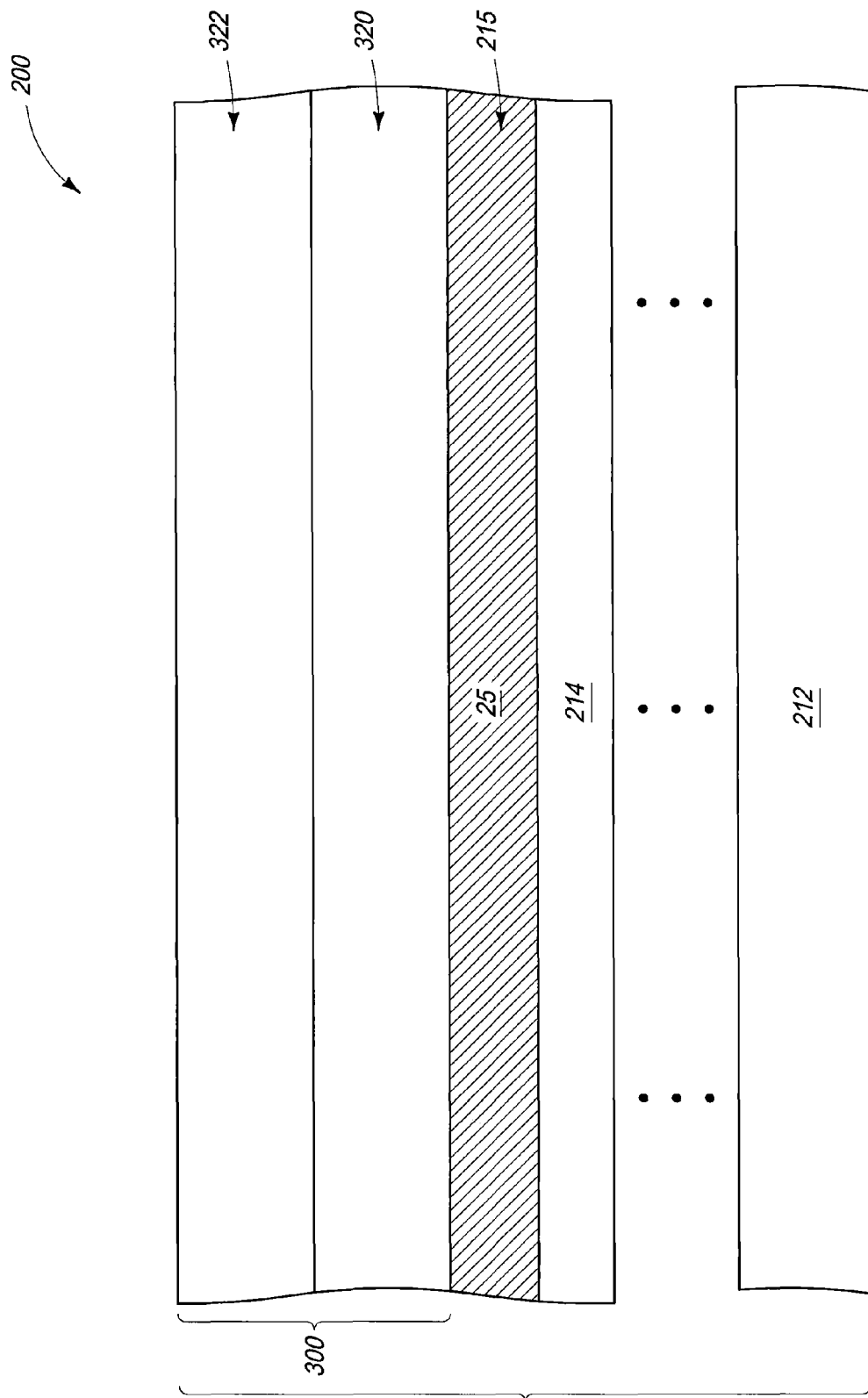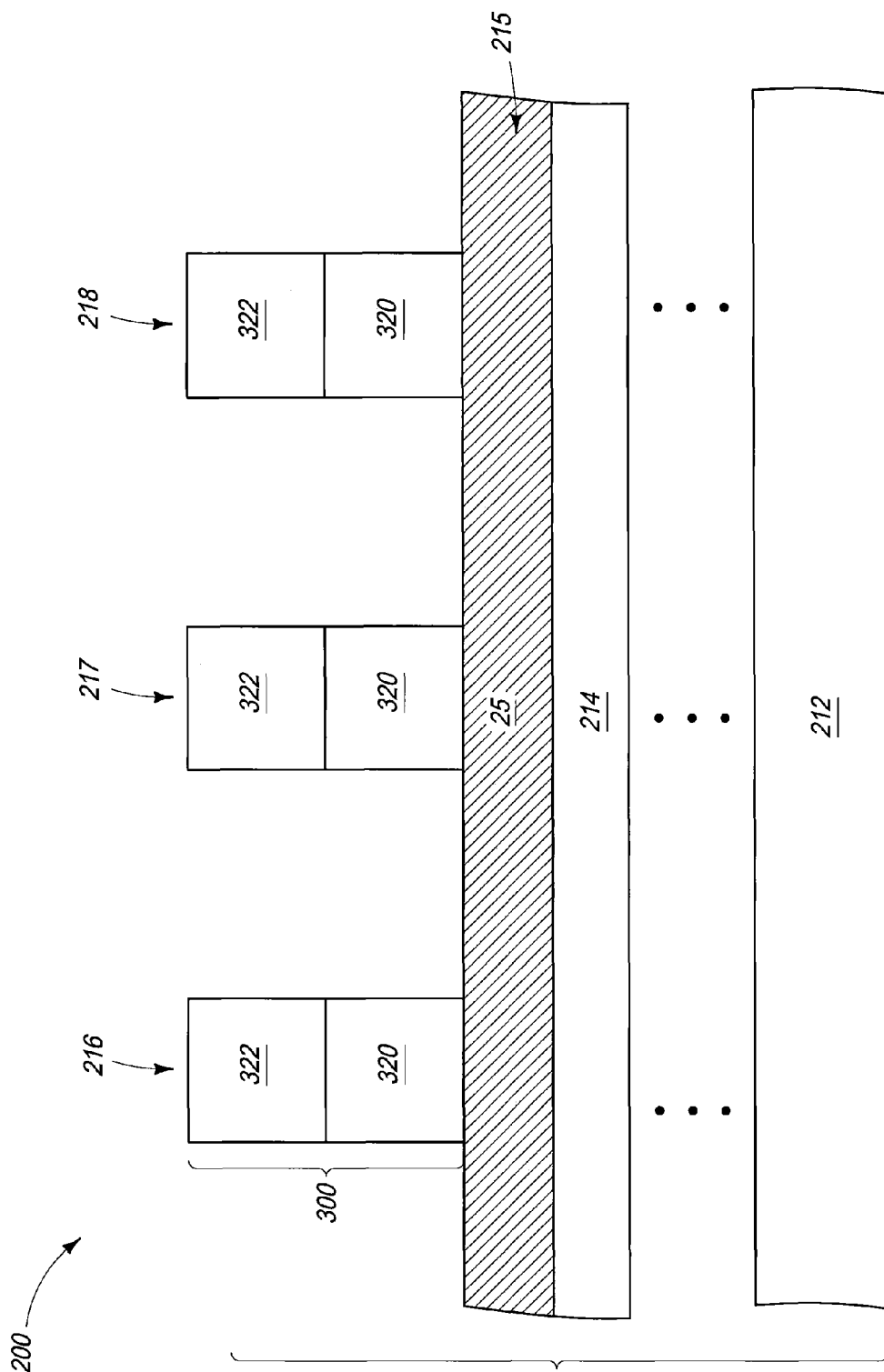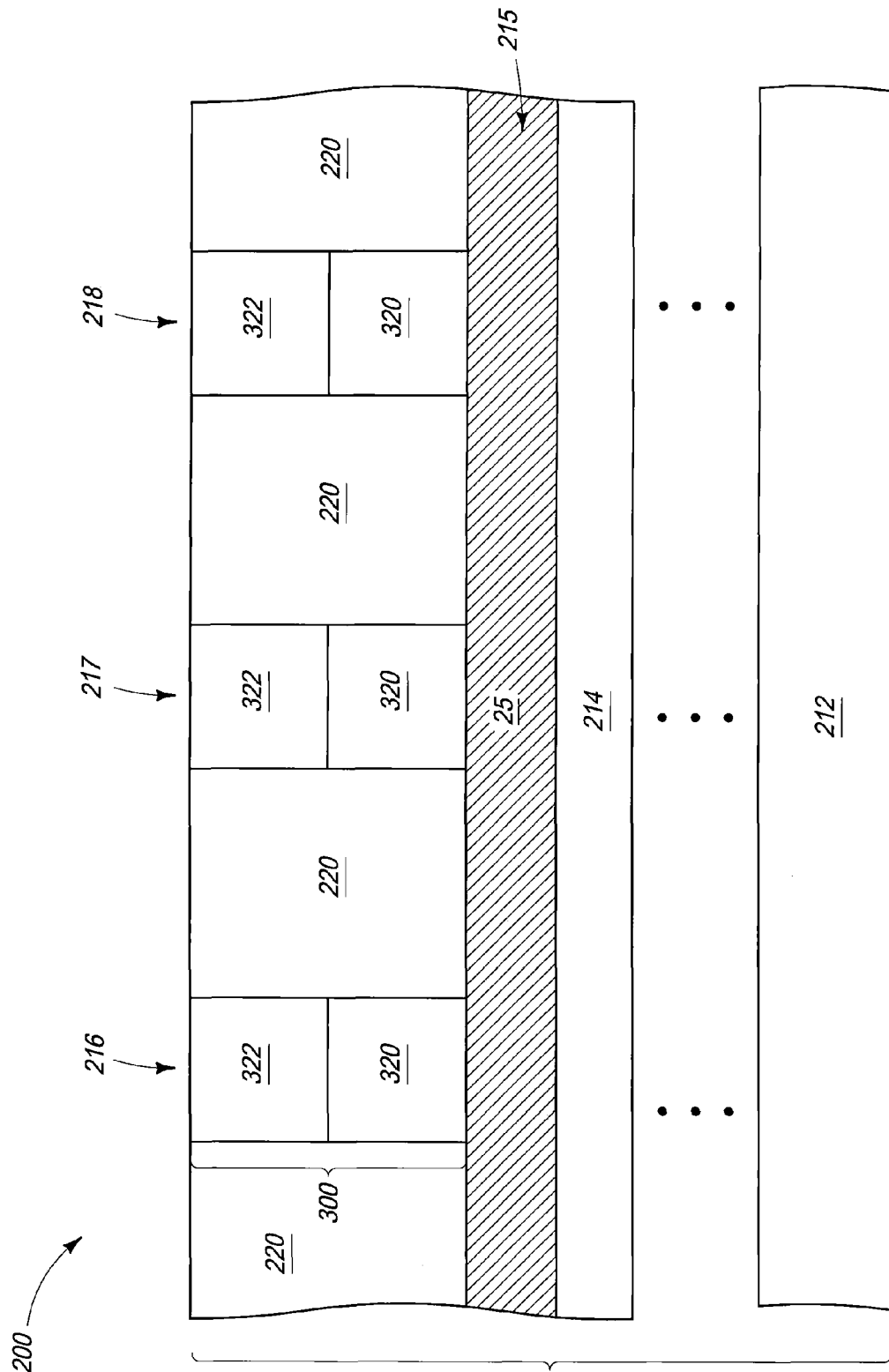25

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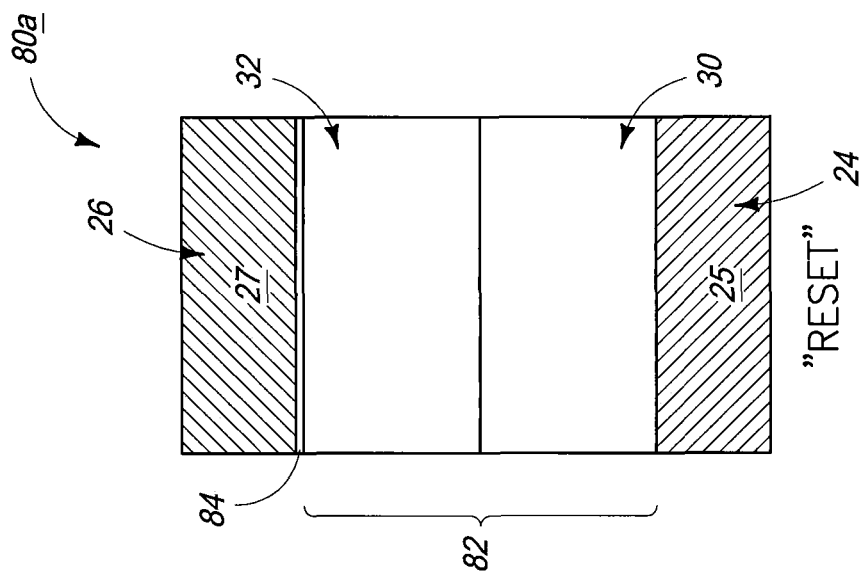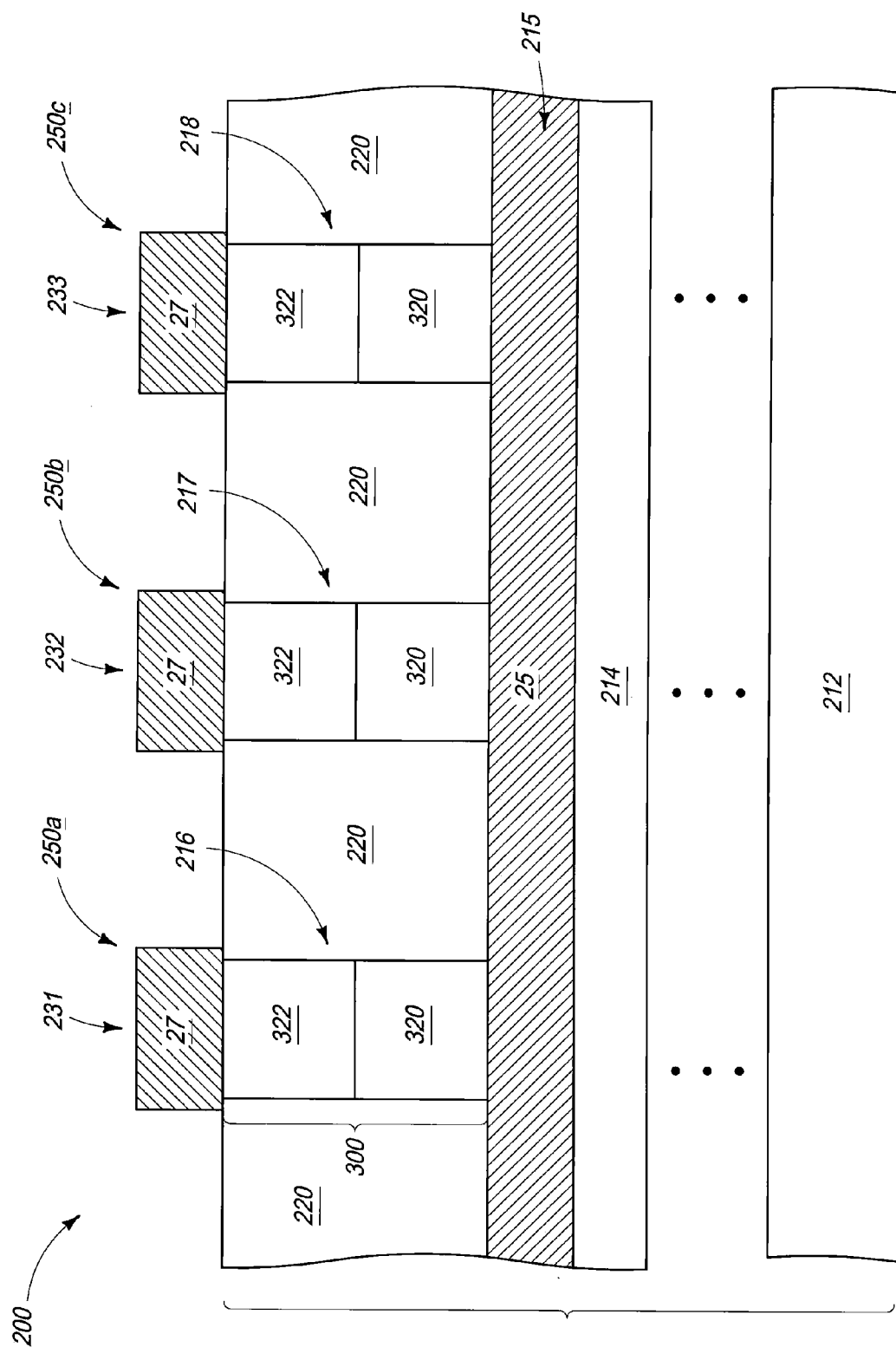
FIG. 15

FIG. 16

FIG. 17

FIG. 18

FIG. 19

MEMORY CELLS, METHODS OF FORMING MEMORY CELLS, AND METHODS OF PROGRAMMING MEMORY CELLS

RELATED PATENT DATA

This patent resulted from a divisional of U.S. patent application Ser. No. 14/173,096, which was filed Feb. 5, 2014, and which is hereby incorporated herein by reference; which resulted from a divisional of U.S. patent application Ser. No. 13/919,677, which was filed Jun. 17, 2013, which issued as U.S. Pat. No. 8,681,531, and which is hereby incorporated herein by reference; which resulted from a divisional of U.S. patent application Ser. No. 13/034,031, which was filed Feb. 24, 2011, which issued as U.S. Pat. No. 8,488,365, and which is hereby incorporated herein by reference.

TECHNICAL FIELD

Memory cells, methods of forming memory cells, and methods of programming memory cells.

BACKGROUND

Memory is one type of integrated circuitry, and is used in computer systems for storing data. Integrated memory is usually fabricated in one or more arrays of individual memory cells. The memory cells may be volatile, semi-volatile, or nonvolatile. Nonvolatile memory cells can store data for extended periods of time, and in some instances can store data in the absence of power. Volatile memory dissipates and is therefore refreshed/rewritten to maintain data storage.

The memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store more than two levels or states of information.

There is a continuing effort to produce smaller and denser integrated circuits. The smallest and simplest memory cell will likely be comprised of two electrically conductive electrodes having a programmable material received between them. Such memory cells may be referred to as cross-point memory cells.

Programmable materials suitable for utilization in cross-point memory will have two or more selectable and electrically differentiable memory states. The multiple selectable memory states can enable storing of information by an individual memory cell. The reading of the cell comprises determination of which of the memory states the programmable material is in, and the writing of information to the cell comprises placing the programmable material in a predetermined memory state. Some programmable materials retain a memory state in the absence of refresh, and thus may be incorporated into nonvolatile memory cells.

Significant interest is presently being directed toward programmable materials that utilize ions as mobile charge carriers. The programmable materials may be converted from one memory state to another by moving the mobile charge carriers therein to alter a distribution of charge density within the programmable materials. Memory devices that utilize migration of mobile charge carriers to transition from one memory state to another are sometimes referred to as Resistive Random Access Memory (RRAM) cells.

A difficulty in utilizing memory cells that simply consist of programmable material received between a pair of electrodes (i.e., cross-point memory cells) is that there can be substantial leakage of current through the devices, and such may

adversely lead to errors during retrieval of stored data from a memory array. Accordingly, diodes or other select devices are commonly paired with the memory cells to assist in control of current through the memory cells. The select devices consume valuable space, and accordingly it would be desirable to develop memory cells which could perform suitably without adjacent select devices.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1-3** are graphical, diagrammatic illustrations of the effect of ion concentration on the conductivity type of some materials.

FIG. **4** shows diagrammatic views of an example embodiment memory cell in a first memory state (a "RESET" state) and a second memory state (a "SET" state), with such memory states being shown to be interchangeable through application of electric field (EF).

FIG. **5** is a graphical illustration of an example curve of current (I) versus voltage (V) characteristics for the memory cell of FIG. **4**.

FIG. **6** is a schematic illustration of an example circuit layout that may be utilized for an array of memory cells having characteristics of the FIG. **4** memory cell.

FIG. **7** shows diagrammatic views of another example embodiment memory cell in a first memory state (a "RESET" state) and a second memory state (a "SET" state), with such memory states being shown to be interchangeable through application of electric field (EF).

FIG. **8** is a graphical illustration of an example curve of current (I) versus voltage (V) characteristics for the memory cell of FIG. **7**.

FIG. **9** shows diagrammatic views of another example embodiment memory cell in a first memory state (a "RESET" state) and a second memory state (a "SET" state), with such memory states being shown to be interchangeable through application of electric field (EF).

FIG. **10** is a graphical illustration of an example curve of current (I) versus voltage (V) characteristics for the memory cell of FIG. **9**.

FIG. **11** shows diagrammatic views of another example embodiment memory cell in a first memory state (a "RESET" state) and a second memory state (a "SET" state), with such memory states being shown to be interchangeable through application of electric field (EF).

FIG. **12** is a diagrammatic view of another example embodiment memory cell.

FIG. **13** shows diagrammatic views of another example embodiment memory cell in a first memory state (a "RESET" state) and a second memory state (a "SET" state), with such memory states being shown to be interchangeable through application of electric field (EF).

FIG. **14** shows diagrammatic views of another example embodiment memory cell in a first memory state (a "RESET" state) and a second memory state (a "SET" state), with such memory states being shown to be interchangeable through application of electric field (EF).

FIGS. **15-19** show diagrammatic cross-sectional views of a portion of a semiconductor construction at various stages of an example embodiment process for fabricating a memory array.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

In some embodiments, the invention includes memory cells which are programmed by altering a concentration of

ions within at least one region of a programmable material. The memory cells may be further configured so that a pn diode forms within the programmable material simultaneously with a transition of the programmable material into a high-conductivity (i.e., low-resistance) memory state. Accordingly, the memory cells may have a pn diode intrinsically formed within a programmable material as the programmable material transitions into a high-conductivity memory state.

As discussed above in the "Background" section of this disclosure, a problem associated with prior art cross-point memory architectures can be that such architectures have select devices external of the memory cells, and paired with each of the memory cells, which increases the space consumed by such architectures. In contrast, some embodiments of the present invention may have a diode intrinsically formed within the programmable material, and may utilize such diode in place of the conventional select devices that would otherwise be formed externally of the memory cell. Such may enable higher integration density to be achieved than is achieved with prior art memory cells.

Some systems are known in which ions may be utilized to induce a conductivity type (specifically, n-type or p-type). FIG. 1 graphically illustrates a system in which a conductivity type is influenced by the concentration of ions (represented as [I]). Specifically, at some ion concentrations the system is in a regime 10 having n-type characteristics, and at other ion concentrations the system is in a regime 14 having p-type characteristics. An intermediate regime 12 is between the regimes 10 and 14, and in such intermediate regime the system may have characteristics which are indeterminate relative to n-type and p-type, or may have other electrical characteristics (such as electrically insulative characteristics), depending on the system.

The system of FIG. 1 is also shown comprising a regime 9 in which the concentration of ions is less than that suitable to induce n-type characteristics, as well as a regime 15 in which the concentration of ions is greater than that which induces p-type characteristics. Either of the regimes 9 and 15 may have conventional electrically insulative characteristics, or conventional electrically conductive characteristics, depending on the system.

FIG. 2 illustrates the same system as FIG. 1, but shown with an alternative convention relative to that of FIG. 1. Specifically, FIG. 2 shows the conductivity type of the system being influenced by the concentration of ion vacancies (represented as $[V_1]$). The concentration of ion vacancies may be roughly inverse to the concentration of ions. Accordingly, FIG. 2 shows the same regions 9, 10, 12, 14 and 15 as FIG. 1, but shows such regions having an inverse relationship relative to the relationship illustrated in FIG. 1. The "vacancies" are typically not empty spaces, but rather are regions where ions could be present, and are not. Such regions may have any of numerous configurations, but are real physical moieties that can have measurable mobility within a system.

A distribution of ions within a material may be described as either the concentration of the ions themselves, or as the concentration of vacancies of the ions. The vacancies will typically have an opposite charge to the ions themselves. In some contexts it is conventional to refer to positively-charged species in a system. In such contexts, it will be the charge which will determine whether a system is described in terms of vacancy concentration or ion concentration. For instance, since oxygen-containing ions typically have a negative charge, it may be preferred to describe the charged species of an oxygen-based system as vacancies in some contexts.

Although the concentration of ion vacancies is sometimes considered as the inverse of the concentrations of ions, there may not be a simple correlation between the concentration of ions and the concentration of ion vacancies in some systems. For instance, there may be differences between ion mobility and ion vacancy mobility which leads to faster accumulation of either ions or vacancies, and thus leads to imbalance between a rate of change in ion concentration relative to a rate of change of ion vacancy concentration. Accordingly, many of the systems described herein may be considered to utilize alteration of either or both of ion concentration and ion vacancy concentration to achieve desired changes within the systems.

FIG. 3 graphically illustrates an oxygen-based system, or, more specifically, a system in which conductivity type is influenced by a concentration of oxygen-containing ions. The concentration of oxygen atoms is approximated in FIG. 3 by the concentration of oxygen-containing ion vacancies (V_O). The system has the same regimes 9, 10, 12, 14 and 15 discussed above with reference to FIGS. 1 and 2. The system of FIG. 3 may contain oxygen ions distributed within a composition that comprises oxygen in combination with one or more of praseodymium, barium, calcium, manganese, strontium, titanium, iron, cesium and lead. For instance, the composition may comprise one or more of PrCaMnO, BaSrTiO, SrTiO, SrCeFeO, and PbO, where such compositions are shown in terms of the elements contained therein, rather than in terms of a specific stoichiometry. In some embodiments, the composition shown as PrCaMnO may correspond to $Pr_{(1-x)}$ Ca_xMnO_3, where x is any number greater than 0 and less than 1.

Oxygen-based systems may be highly sensitive to the concentration of oxygen-containing ions (and/or to the concentration of vacancies of oxygen-containing ions). For instance, a change in the concentration of oxygen ions of about 10 parts per million may shift SrTiO from the regime 10 having n-type characteristics to the regime 14 having p-type characteristics.

The oxygen-based systems represented by FIG. 3 may be considered to correspond to valence change material systems. Specifically, the systems comprise materials having one or more elements with multiple stable valence states (for instance, titanium, iron, manganese, etc.). Valence change systems are example systems that may be utilized in some embodiments. Valance change systems may comprise mobile ions, and/or mobile ion vacancies, that can be moved within the systems to alter ion and ion vacancy concentrations throughout the systems. Mobile ions and mobile ion vacancies may or may not coexist in a single system, depending on the system. Thus, one or both of the mobile species corresponding to mobile ions and mobile ion vacancies may be utilized to alter ion concentration, and/or ion vacancy concentration, within a given system.

Oxygen-based systems of the type represented in FIG. 3 are examples of the types of systems that may be utilized in various embodiments of the invention. Any suitable systems may be utilized, and other example systems are sulfur-based systems, nitrogen-based systems, etc.

The curves of FIGS. 1-3 are qualitative representations of the relationship between ion concentration (and/or ion vacancy concentration) and conductivity type for various systems. The concept being illustrated is that the conductivity type of some systems may be influenced and changed by an ion concentration (and/or an ion vacancy concentration) within such systems. Actual systems may have a different relationship between the ion concentration (and/or the ion vacancy concentration) and the conductivity type besides the simple linear curves of FIGS. 1-3. However, as long as an ion

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concentration (and/or the ion vacancy concentration) within a system can influence and alter the conductivity type of the system, such system may be suitable for incorporation into the programmable material of memory cells in various aspects of the present invention.

FIG. 4 illustrates an example memory cell 20 having a programmable material 22 sandwiched between a pair of electrodes 24 and 26. In some embodiment, the memory cell may be considered to be an example of a bipolar switching RRAM diode cell.

The electrodes 24 and 26 comprise electrically conductive materials 25 and 27, respectively. The materials 25 and 27 may comprise any suitable electrically conductive compositions or combinations of compositions; and in some embodiments may comprise one or more of various metals, metal-containing compositions, and conductively-doped semiconductor materials. The materials 25 and 27 may be compositionally the same as one another in some embodiments, and may be compositionally different from one another in other embodiments.

In some embodiments, the electrode 24 may be part of a first linear segment that extends along a first direction (analogous to a first linear segment described below with reference to FIG. 19), and the electrode 26 may be part of a second linear segment that extends along a second direction that crosses the first direction (analogous to one of the second linear segments described below with reference to FIG. 19). The memory cell 20 is formed at a location where the first and second linear segments overlap one another, and comprises the programmable material 22 directly between the first and second linear segments.

The programmable material 22 comprises two regions 30 and 32 which are compositionally different from one another, and which may both have characteristics of the various systems described above with reference to FIGS. 1-3. For instance, the regions 30 and 32 may comprise any of the various oxygen-based systems described with reference to FIG. 3. The compositional difference between regions 30 and 32 may be substantial, such as having a composition of one of the regions comprising one or more elements which are not common to the composition of the other of the regions. Alternatively, the compositional difference between regions 30 and 32 may be subtle, such as having the same mixture of elements within both regions, and having a stoichiometric difference between the regions. In any event, in some embodiments the difference between regions 30 and 32 is more than a transitory difference, and thus more than a mere difference in the population of ions between the two regions. The interface between the layers 30 and 32 may be abrupt in some embodiments, diffuse in some embodiments, and/or may comprise a gradient in some embodiments. Although regions 30 and 32 are described as being compositionally different than one another, in other embodiments the difference between regions 30 and 32 may be solely due to different concentrations of ions within the regions as induced by a programming operation.

Although the shown programmable material 22 has two different regions, in other embodiments a programmable material may have more than two different regions. If the programmable material has more than two different regions, all of the regions may be compositionally different from one another; or two or more of the regions may be compositionally the same as one another, and spaced from one another by at least one region which is compositionally different from them.

The regions 30 and 32 are shown to be directly against one another. In other embodiments the regions may be spaced from one another by intervening materials or regions. For instance, an embodiment discussed below with reference to FIG. 11 comprises an insulating material between the regions 30 and 32.

The regions 30 and 32 may comprise any suitable thicknesses, and may be about the same thickness as one another (as shown), or may be different thicknesses relative to one another. In some embodiments, each of the regions 30 and 32 may have a thickness of from about 5 nanometers to about 100 nanometers.

In the example embodiment FIG. 4, each of the regions 30 and 32 comprises a system which can be changed from one conductivity type to another by altering a concentration of ions (and/or ion vacancies) within the system. Both systems are influenced by the same ions (and/or ion vacancies), and thus the relative conductivity types of regions 30 and 32 may be tailored by altering the relative concentration of the ions (and/or ion vacancies) within the two regions 30 and 32.

The distribution of the ions and ion vacancies across programmable material 22 is diagrammatically indicated along the sides of the programmable material with arrows 31 and 33. Specifically, arrow 31 indicates that a concentration of ions ([I]) increases along one direction through the programmable material, and arrow 33 indicates that there is an increase in vacancies of the ion ($[V_1]$) in a direction opposite to the direction of the arrow 31.

The embodiment of FIG. 4 shows the region of programmable material having a high concentration of ions (or alternatively, a low concentration of ion vacancies) being p-type, and shows the region of the programmable material having the low concentration of ions (or alternatively, a high concentration of ion vacancies) being n-type. Such relationship of ion concentration (or ion vacancy concentration) to conductivity type is consistent with the oxygen-based systems described above with reference to FIG. 3. In other embodiments, other systems may be utilized, and the relationship of conductivity to ion concentration (or ion vacancy concentration) may be opposite to that shown in FIG. 4 (e.g., a high ion concentration, or low ion vacancy concentration, may correspond to an n-type region rather than corresponding to the p-type region shown in FIG. 4).

FIG. 4 shows memory cell 20 in two different interchangeable memory states, which are designated as a "RESET" state and a "SET" state. The regions 30 and 32 are of opposite conductivity type relative to one another in both of the "RESET" and "SET" memory states.

The two memory states of FIG. 4 are interchanged with one another by subjecting memory cell 20 to appropriate electric fields. An electric field oriented along a first direction (the field designated as $EF^{(+)}$ in FIG. 4) may shift the ion distribution (and/or the ion vacancy distribution) within the memory cell to cause the memory cell to transition from the "RESET" state to the "SET" state. An electric field oriented along a second direction opposite to that of the first direction (the field designated as $EF^{(-)}$ in FIG. 4) may shift the ion distribution (and/or the ion vacancy distribution) within the memory cell to cause the memory cell to transition from the "SET" state to the "RESET" state.

The "RESET" memory state has a pn diode in one orientation, and the "SET" memory state has a pn diode in an opposite orientation relative to that of the "RESET" state. In some embodiments, the regions 30 and 32 may be referred to as first and second regions, and the conductivity types of such regions in the "SET" state may be referred to as first and second conductivity types, respectively; with the first and second conductivity types being opposite to another. In such embodiments, the conductivity type of the first region 30 is

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transitioned from the first conductivity type (shown as n-type), to the second conductivity type (shown as p-type) in changing the memory cell from the "SET" state to the "RESET" state; and the conductivity type of the second region 32 is transitioned from the second conductivity type to the first conductivity type in changing the memory cell from the "SET" state to the "RESET" state. It is noted that the pn diodes of the "SET" and "RESET" memory states are formed within the programmable material 22 simultaneously with the programming of the memory cell into such memory states.

The embodiment of FIG. 4 has conductivity types of the first and second regions 30 and 32 of the "SET" state induced by changes in concentrations of ions (and/or by changes in concentrations of ion vacancies) within each of such regions. In other embodiments (for instance, embodiments discussed below with reference to FIGS. 13 and 14), one of the regions of the programmable material may have a static conductivity type (i.e., a conductivity type which is not changed in transitioning between the "RESET" and "SET" memory states). Accordingly, if the programmable material has two regions, it may be only one of such regions that has a conductivity type induced by a change in a concentration of ions (and/or by a change in a concentration of ion vacancies).

In some embodiments, the reading of the memory cell 20 of FIG. 4 comprises determination of the amount of current passed through the memory cell when an electric field is provided across the programmable material. It is noted that the conditions utilized to transition the memory cell from one memory state to another will use some suitable combination of a sufficient magnitude of electric field, coupled with a sufficient duration of time to enable redistribution of ions (and/or ion vacancies) within the programmable material. The conditions utilized during the reading operation may be chosen to have one or both of the magnitude of electric field and the duration of time that the field is applied to be too low to transition the memory cell from one memory state to another.

The electric field utilized to read the memory cell may be applied along a direction which forward biases the pn diode of the "SET" memory state, and reverse biases the pn diode of the "RESET" memory state. Accordingly, memory cells in the "SET" memory state will pass greater current then memory cells in the "RESET" memory state, and thus may be distinguished from the memory cells in the "RESET" memory state.

In the embodiment of FIG. 4, the ions (and/or ion vacancies) utilized for transitioning the memory cell from one state to another may be contained entirely within the programmable material, and diffused from one region to another during the programming of the memory cell. In such embodiments, barriers may be provided entirely around the programmable material 22 to trap the ions (and/or the ion vacancies) within the programmable material. In some embodiments, the electrodes 24 and 26 may comprise material which blocks diffusion of ions (and/or ion vacancies) therethrough (i.e., which is impermeable to the ions or ion vacancies), and may be directly against the programmable material. In some embodiments, one or more layers of barrier material (not shown) may be provided between the electrodes and the programmable material, and/or along the sides of the programmable material. Example barrier materials which may be used to block diffusion of oxygen-containing ions are described in U.S. Patent Publication No. 2010/0237442, as well as in U.S. Pat. Nos. 6,524,867, 7,727,908, 7,273,791, 7,393,785, 7,544,987 and 7,560,815. Example electrically conductive materials which may block diffusion of oxygen-containing ions, and which may be utilized in electrodes in some embodiments can include, for example, Al, Ir, Ru, RuTiN, RuTiO, RuO—Ta, CeO—Ta, TaN, etc., where such materials are shown in terms of the elements contained therein, rather than in terms of a specific stoichiometry.

If one or both of the electrodes 24 and 26 is spaced from the programmable material 22 by a barrier material (for instance, an oxygen ion-barrier material and/or an oxygen-ion-vacancy barrier material), the barrier material may be electrically insulative or electrically conductive. If the barrier material is electrically insulative, it may be formed to be thin enough that current can still pass through the barrier material during reading and programming of the memory cell. If the barrier material is electrically conductive, it may be considered to be comprised by the electrode that is directly adjacent to the barrier material.

FIG. 5 shows a "current vs. voltage" curve illustrating performance characteristics of the memory cell 20 of FIG. 4. The curve has four important events which are specifically labeled along such curve.

The event (1) corresponds to an increase in voltage while the memory cell remains in the "RESET" memory state.

The next event (2) corresponds to a transition that occurs when the voltage reaches a level Vset, whereupon the pn diode of the "RESET" memory state is reversed to transition the memory cell into the "SET" memory state. It is noted that the current flow through the "SET" memory state is cut-off (i.e., truncated) at a level 35. Such truncation represents a current cut-off provided for current compliance to protect semiconductor devices. In theory, such cut-off would not exist for an idealized memory device utilized in the absence of other circuitry, but in practice it is generally utilized.

The next event (3) corresponds to a decrease in voltage while the memory device remains in the "SET" memory state. There is a voltage level indicated as Vt1, which is below the level Vset, but at which substantial current flows through the memory cell in the "SET" memory state. Such level may correspond to a suitable voltage level for reading the memory device without inadvertently tripping the device into the "SET" or "RESET" memory state.

The next event (4) corresponds to a transition that occurs when the voltage reaches a level Vreset, whereupon the pn diode of the "SET" memory state is reversed to transition the memory cell into the "RESET" memory state. The current flow through the "RESET" memory state may be cut-off at a level 37 for the current compliance reasons discussed above relative to the cut-off level 35.

The "RESET" memory state of the memory cell 20 of FIG. 4 may be exactly the opposite of the "SET" memory state of such memory cell. Accordingly, reading of the memory cell may comprise utilization of electric field oriented such that the pn diode of the "RESET" is forward biased, while the pn diode of the "SET" state is reverse biased. Such read operation is diagrammatically illustrated in FIG. 5 by indicating a voltage level Vt2 which could be utilized analogously to the above-discussed voltage level Vt1, but which would forward bias the pn diode of the "RESET" memory state.

It can be advantageous that the memory cell 20 of FIG. 4 has the two different and opposite read operations which may be accomplished by either forward biasing the pn diode of the "SET" memory state or the pn diode of the "RESET" memory state. For instance, such can provide additional flexibility for design of read operations to be utilized for ascertaining the memory states of the various memory cells in a memory cell array. However, in some embodiments it is also acceptable to use only one read operation to distinguish the two states.

The memory cell 20 of FIG. 4 has an intrinsic pn diode within the programmable material after the programmable

material is transitioned into a memory state. Such intrinsic diode may eliminate the need for the extrinsic diodes (or other select devices) paired with the cross-point memory cells. FIG. 6 shows a schematic diagram of a portion of a memory array 38. Such memory array comprises a plurality of cross-point memory cells 20a-20i. The memory array also comprises a series of first access lines 40-42 extending along a first direction, and a series of second access lines 43-45 extending along a second direction, and intersecting with the first access lines. The memory cells 20a-20i are provided at locations where the first access lines intersect the second access lines, and thus each memory cell may be uniquely addressed through the combination of a first access line and a second access line.

FIG. 6 shows that voltages of ½ unit, 0 unit and ½ unit, respectively are along the access lines 40, 41 and 42; and that voltages of ½ unit, 1 unit and ½ unit, respectively are along access lines 43, 44 and 45. In the shown configuration, the memory cell 20e will experience an electric field of 1 unit, which will be significantly larger than the electric field experienced by any of the other memory cells. For instance, memory cells 20a, 20c, 20g and 20i may experience electric fields of about 0 units, while the memory cells 20b, 20d, 20f and 20h may experience electric fields of about ½ unit. Thus, the memory cell 20e may be uniquely addressed for programming, and similarly may be uniquely addressed for reading. Each of the other of memory cells may be analogously uniquely addressed for programming and reading. The programming voltage utilized for programming the memory cells of FIG. 6 may be, for example, from about 1 volt about 4 volts.

FIG. 7 shows an example embodiment memory cell 50, which is different than the example embodiment memory cell 20 of FIG. 4. In referring to FIG. 7, similar numbering will be used as is used above in describing the memory cell of FIG. 4, where appropriate.

The memory cell 50 has a programmable material 52 sandwiched between the pair of electrodes 24 and 26. The programmable material comprises two regions 60 and 62 which are compositionally different from one another. One or both of the regions may comprise a system which changes conductivity type depending upon the concentration of ions (and/or depending on the concentration of ion vacancies) within such system. For instance, one or both of the regions may comprise a system of any of the types described above with reference to FIGS. 1-3.

The memory cell 50 is shown to have interchangeable "RESET" and "SET" memory states; with such states being interchanged using the electric fields EF$^{(+)}$ and EF$^{(-)}$.

The "SET" memory state is similar to the "SET" memory state of the FIG. 4 memory cell, and accordingly comprises a pn diode within the programmable material 52. Further, the "SET" state of memory cell 50 is shown to have ions (or vacancies) diffused within both of the regions 60 and 62. The arrows 31 and 33 are provided along the memory cell in the "SET" memory state to illustrate that an ion concentration increases along a direction from region 60 to 62, and that an ion vacancy concentration increases along a direction from region 62 to 60. The shown embodiment has a p-type region at high levels of the ion concentration (or alternatively considered, at low levels of the ion vacancy concentration); and has an n-type region at low levels of the ion concentration (or alternatively considered, at high levels of the ion vacancy concentration). In other embodiments, the relative dependence on the ion concentration (or ion vacancy concentration) of the p-type and n-type regions may be reversed—i.e., the n-type region may occur at high concentrations of the ions (or

low concentrations of ion vacancies), and the p-type region may occur at low concentrations of the ions (or high concentrations of ion vacancies).

The regions 60 and 62 in the "RESET" memory state of the memory cell are not labeled relative to n-type and p-type. In some embodiments, one or both of the regions 60 and 62 may have electrically insulative properties in the "RESET" memory state. For instance, one or both of the regions 60 and 62 may have ions (or vacancies) diffused therein to a concentration corresponding to the regime 12 of FIGS. 1-3. Such regime is neither n-type nor p-type, and in some embodiments may have characteristics of electrically insulative material. Alternatively, the electrically insulative regime may occur in one or both of the regimes 9 and 15 of FIGS. 1-3 when the ion concentration (or ion vacancy concentration) is outside of appropriate concentrations for the n-type and p-type regimes 10 and 14.

Although neither of the regions 60 and 62 of the "RESET" state is specifically labeled as n-type or p-type, in some embodiments one of the regions may be n-type or p-type, while the other is electrically insulative. For instance, region 60 may be n-type or p-type, while region 62 is electrically insulative; or vice versa.

In an example embodiment in which region 60 is p-type and region 62 is electrically insulative, the transition to the "SET" memory state comprises changing conductivity of both regions. Specifically, region 62 is changed from electrically insulative to p-type, and region 60 is changed from p-type to n-type.

In an example embodiment in which region 60 is n-type and region 62 is electrically insulative, the transition to the "SET" memory state comprises changing conductivity of only region 62. Specifically, region 62 is changed from electrically insulative to p-type, while region 60 remains n-type.

Even though region 60 may remain n-type in both the "RESET" and "SET" memory states of the memory cell, the concentration of ion vacancies within region 60 may increase (and/or the concentration of ions may decrease) in going from the "RESET" memory state to the "SET" memory state. For instance, regions 60 and 62 may comprise different systems, with the system of region 62 needing a higher concentration of ion vacancies (and/or a lower concentration of ions) to transition into a p-type regime than does the region 60. Thus, in the "RESET" memory state the region 60 may be n-type even though it has a significant ion concentration (and/or has a low concentration of ion vacancies). Subsequently, the transition into the "SET" state may comprise diffusion of ions from region 60 into region 62 (and/or diffusion of ion vacancies from region 62 to region 60), and there may be enough ions (and/or ion vacancies) migrating between regions 60 and 62 to convert the system of region 62 into the p-type regime. As another example, regions 62 and 60 may comprise similar systems, but region 62 may be much thinner than region 60. Thus, even though the concentration of ions and/or vacancies within the region 60 is insufficient to achieved the necessary concentration to convert the thick region 60 into the p-type regime in the "RESET" memory state, there are enough ions and/or ion vacancies migrating between the thick region 60 and the thin region 62 during the transition to the "SET" memory state to convert region 62 into the p-type regime. Alternatively, region 60 may be an n-type semiconductor material that is not affected by the ion concentration (or ion vacancy concentration), analogously to constructions discussed below with reference to FIG. 13.

FIG. 8 shows a "current vs. voltage" curve illustrating performance characteristics of the memory cell 50 of FIG. 7. The curve has four important events which are specifically

labeled along such curve, with such events being analogous to the events described above with reference to the "current vs. voltage" curve of FIG. 5.

The event (1) corresponds to an increase in voltage while the memory cell remains in the "RESET" memory state. In the shown embodiment, the programmable material 52 (FIG. 7) has at least one electrically insulative region (i.e., at least one of the regions 60 and 62 of FIG. 7 is electrically insulative in the "RESET" state), and thus no current flows through the memory cell while the cell is in the "RESET" state.

The next event (2) corresponds to a transition that occurs when the voltage reaches a level Vset, whereupon the pn diode of the "SET" memory state is formed. The current flow through the "SET" memory state has the cut-off at level 35 discussed above with reference to FIG. 5.

The next event (3) corresponds to a decrease in voltage while the memory device remains in the "SET" memory state. There is a voltage level indicated as Vt1 analogous to the level Vt1 discussed above with reference to FIG. 5. Such level may correspond to a suitable voltage level for reading the memory device.

The next event (4) corresponds to a transition that occurs when the voltage reaches a level Vreset, whereupon the at least one insulative region is reformed, and current ceases to flow through the memory device.

FIG. 9 shows another example embodiment memory cell 70. The memory cell 70 is equivalent to the memory cell 50 of FIG. 7, but inverted relative to the memory cell of FIG. 7.

The memory cell 70 has the programmable material 52 sandwiched between the pair of electrodes 24 and 26. The programmable material comprises the two regions 60 and 62 described above.

The memory cell 70 has the interchangeable "RESET" and "SET" memory states described above with reference to FIG. 7. However, the pn diode within the "SET" memory state of FIG. 9 is inverted relative to that of FIG. 7. Arrows 31 and 33 are provided in FIG. 9 along the memory cell in the "SET" memory state to illustrate that an ion concentration increases along a direction from region 62 to 60, and that an ion vacancy concentration increases along a direction from region 60 to 62.

Like the embodiment of FIG. 7, neither of the regions 60 and 62 of the "RESET" state of FIG. 9 is specifically labeled as n-type or p-type. In some embodiments both of the regions 60 and 62 may be electrically insulative in the "RESET" state of FIG. 9; and in other embodiments one of the regions may be n-type or p-type, while the other is electrically insulative. For instance, region 60 may be n-type or p-type, while region 62 is electrically insulative.

In an example embodiment in which region 60 is n-type and region 62 is electrically insulative, the transition to the "SET" memory state comprises changing conductivity of both regions. Specifically, region 62 is changed from electrically insulative to n-type, and region 60 is changed from n-type to p-type. Such may comprise diffusing ions (or vacancies) from the insulative region 62 of the "RESET" memory state into the region 60 to transition to the "SET" memory state.

In an example embodiment in which region 60 is p-type and region 62 is electrically insulative, the transition to the "SET" memory state comprises changing conductivity of only the region 62. Specifically, region 62 is changed from electrically insulative to n-type, while region 60 remains p-type. Such may comprise diffusing ions (or vacancies) between the regions 60 and 62. The shown configuration is an example configuration in which regions with a relatively high ion concentration (and a relatively low ion vacancy concen-

tration) are p-type, and regions with a relatively low ion concentration are n-type (and a relatively high ion vacancy concentration).

FIG. 10 shows a "current vs. voltage" curve illustrating performance characteristics of the memory cell 70 of FIG. 9. The curve has four important events which are specifically labeled along such curve, with such events being analogous to those described above with reference to FIG. 8, but of opposite orientation relative to those of FIG. 8.

The event (1) of FIG. 10 corresponds to a decrease in voltage while the memory cell remains in the "RESET" memory state.

The next event (2) corresponds to a transition that occurs when the voltage reaches a level Vset, whereupon the pn diode of the "SET" memory state is formed.

The next event (3) corresponds to an increase in voltage while the memory device remains in the "SET" memory state. There is a voltage level indicated as Vt1 analogous to the level Vt1 discussed above with reference to FIG. 8, which may correspond to a suitable voltage level for reading the memory device.

The next event (4) corresponds to a transition that occurs when the voltage reaches a level Vreset, whereupon the at least one insulative region is reformed, and current ceases to flow through the memory device.

FIG. 11 shows another example embodiment memory cell 80 with interchangeable "RESET" and "SET" memory states. In referring to FIG. 11, similar numbering will be used as is used above in describing the memory cell of FIG. 4, where appropriate.

The memory cell 80 has a programmable material 82 between the pair of electrodes 24 and 26. The programmable material 82 comprises the two regions 30 and 32 described above with reference to the memory cell 20 of FIG. 4. However, the memory cell 80 differs from the memory cell 20 of FIG. 4 in that the memory cell 80 comprises an ion (and/or ion vacancy) reservoir 84 between the regions 30 and 32. The reservoir 84 may comprise electrically conductive material in some embodiments, and may comprise electrically insulative material in some embodiments.

In some embodiments, the ions may be oxygen-containing species, and accordingly the reservoir may be a material which contains an excess of oxygen-containing species in at least one of the memory states. For instance, the reservoir may be an insulative material comprising oxygen-enriched oxide (such as silicon oxide, aluminum oxide, etc.) in at least one of the memory states. The reservoir may be permeable to the ions (and/or to the ion vacancies) in some embodiments.

The ion (and/or ion vacancy) reservoir may be kept very thin so that it does not substantially interfere with current flow through the programmable material in the "SET" memory state, and in example embodiments may have a thickness of less than or equal to about 50 angstroms, less than or equal to about 20 angstroms, or any other suitable thickness.

The reservoir may act as a source of ions (and/or ion vacancies) for altering one or both of ion density and ion vacancy density in one of the regions of the programmable material during a transition from the "RESET" memory state to the "SET" memory state, or vice versa; and/or may act as a sink for excess ions, or ion vacancies, during transitioning from one memory state to the other. In some embodiments, the reservoir may facilitate movement of ions (and/or ion vacancies), which may facilitate rapid switching from one memory state to another, and may thus improve one or both of reading speed and writing speed.

The reservoir 84 may be placed in any suitable location within the programmable material, and in some embodiments

there may be more than one reservoir of ions (and/or ion vacancies) provided within the programmable material. In the shown embodiment, the reservoir **84** is between the regions **30** and **32**, and directly against both of such regions. In other embodiments, the reservoir may be placed in other locations.

FIG. **12** illustrates example embodiment memory cell **80***a* analogous to the memory cell **80** of FIG. **11**, but comprising the reservoir **84** along a top of the programmable material, rather than in a middle of the programmable material; and specifically directly between the region **32** and the top electrode **26**. As noted above, in some embodiments the reservoir **84** may correspond to an electrically conductive material. Accordingly, in some embodiments the memory cell of FIG. **12** may be considered to comprise an electrically conductive material **84** directly between the top electrode **26** and the top region **32** of the programmable material.

FIG. **13** shows another example embodiment memory cell **90** with interchangeable "RESET" and "SET" memory states. In referring to FIG. **13**, similar numbering will be used as is used above in describing the memory cell of FIG. **4**, where appropriate.

The memory cell **90** has a programmable material **92** between the pair of electrodes **24** and **26**. The programmable material comprises two regions **94** and **96** which are compositionally different from one another. The region **94** comprises p-type doped semiconductor material (for instance, p-type doped silicon) while the region **96** comprises a system which changes conductivity type depending upon the concentration of ions, or ion-vacancies, within such system. For instance, the region **96** may comprise a system of any of the types described above with reference to FIGS. **1-3**. The conductivity of the doped semiconductor material of region **94** does not change in transitioning between the "RESET" memory state and the "SET" memory state, and in the shown embodiment remains p-type in both memory states.

The region **96** is shown to have n-type conductivity in the "SET" memory state, so that regions **94** and **96** together form a pn diode in the "SET" memory state.

The region **96** may have electrically insulative properties in the "RESET" state, and an electric field which forward biases the pn diode of the "SET" may be utilized to distinguish the "RESET" memory state from the "SET" memory state.

In the shown embodiment, ions (or vacancies) within programmable material **92** are only within the region **96** in both the "RESET" and "SET" memory states (as indicted by the concentration of ions ([I]) being shown only within the region **96** in FIG. **13**). Accordingly, region **94** of the programmable material does not act as a reservoir of ions or vacancies during the transition between the "RESET" and "SET" memory states. Rather, electrode **26** may be configured to be permeable to the ions (and/or vacancies), so that ions (and/or vacancies) may pass through such electrode during transitioning between the "RESET" memory state and the "SET" memory state. Any suitable electrically conductive material permeable to the ions and/or vacancies may be utilized for the electrode **26**. Example materials which are permeable to oxygen-containing ions may include Pt and/or materials described in U.S. Pat. No. 7,273,791.

The region **96** has a first concentration of ions and/or vacancies, shown as $[I]_1$, in the "RESET" memory state; and a second concentration of ions and/or vacancies, shown as $[I]_2$, in the "SET" memory state. The second concentration of ions and/or vacancies is different than the first concentration, and such difference leads to the change in conductivity of the region **96** in transitioning from the "RESET" memory state to the "SET" memory state. In some embodiments the concen-

tration $[I]_1$ may be about 0 ions per unit volume, and in other embodiments it may be larger than 0 ions per unit volume.

Although the upper region **96** is shown to be the region which is altered in response to concentration of ions and vacancies in the embodiment of FIG. **13**, in other embodiments it may be the lower region **94** which is altered while the upper region **96** is the conductively-doped semiconductor material. Also, although the p-type doped region of the memory cell is shown to be the region corresponding to doped semiconductor material, in other embodiments it may be the n-type region which corresponds to doped semiconductor material. For instance, an embodiment analogous to that of FIG. **13** has region **96** corresponding to n-type doped semiconductor material, and region **94** corresponding to a system which is in an insulative regime in the "RESET" memory state, and then transitions to the p-type regime in the "SET" memory state due to migration of ions (and/or vacancies) from or to such system.

FIG. **14** shows another example embodiment memory cell **100** with interchangeable "RESET" and "SET" memory states. In referring to FIG. **14**, similar numbering will be used as is used above in describing the memory cell of FIG. **4**, where appropriate.

The memory cell **100** has a programmable material **102** between the pair of electrodes **24** and **26**. The programmable material comprises two regions **104** and **108** which are compositionally different from one another. The region **104** comprises p-type doped semiconductor material (for instance, p-type doped silicon) while the region **108** comprises a system which changes conductivity type depending upon the concentration of ions and/or vacancies within such system. For instance, the region **108** may comprise a system of any of the types described above with reference to FIGS. **1-3**. The conductivity of the doped semiconductor material of region **104** does not change in transitioning between the "RESET" memory state and the "SET" memory state, and in the shown embodiment remains p-type in both memory states.

The memory cell **100** may be fabricated with any suitable methodology. For instance, the construction may be fabricated by providing the material **108** over region **104**. The region **106** may be formed during switching from the "RESET" to "SET" state—as a push (or growth) of a conductive filament through the material **108**, and may be removed during switching from the "SET" to "RESET" state by dissolving the conductive filament.

The region **108** has a first concentration of ions and/or ion-vacancies (shown as $[I]_1$) in the "RESET" memory state, and the region **106** has a second concentration of ions and/or ion-vacancies (shown as $[I]_2$) in the "SET" memory state. The second concentration is different than the first concentration, and such difference leads to formation of the filamentous region **106** in transitioning from the "RESET" memory state to the "SET" memory state. In some embodiments, the concentration $[I]_1$ may be about 0 ions per unit volume, and in other embodiments it may be larger than 0 ions per unit volume.

The memory cell **100** may be operated identically to the memory cell **90** discussed above with reference to FIG. **13**. Notably, the filamentous region **106** directly contacts both the p-type region **104** and the upper electrode **26** in the shown embodiment.

The memory cell **100** is an example memory cell having a first conductivity type filament extending between an electrode and a second conductivity type region, and other similar memory cells may be formed in other embodiments. For instance, in some embodiments, the region **104** may be n-type doped semiconductor material, and thus may be statically

n-type in transitioning between the "RESET" memory state and the "SET" memory state. In such embodiments, the filamentous region **106** may be p-type.

Any suitable process may be utilized to form the various memory cells discussed above with reference to FIGS. **1-14**. An example process for forming an array of memory cells is described with reference to FIGS. **15-19**.

Referring to FIG. **15**, a construction **200** is shown to comprise a base **212**, an electrically insulative material **214** over the base, and a line **215** of the electrically conductive electrode material **25** over such electrically insulative material.

The base **212** may comprise, consist essentially of, or consist of monocrystalline silicon, and may be referred to as a semiconductor substrate, or as a portion of a semiconductor substrate. The terms "semiconductive substrate," "semiconductor construction" and "semiconductor substrate" mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Although base **212** is shown to be homogenous, the base may comprise numerous materials in some embodiments. For instance, base **212** may correspond to a semiconductor substrate containing one or more materials associated with integrated circuit fabrication. In such embodiments, such materials may correspond to one or more of refractory metal materials, barrier materials, diffusion materials, insulator materials, etc.

The electrically insulative material **214** is shown to be spaced from the base **212** by other levels of integrated circuitry. Such levels may include logic, wiring, memory, etc. Alternatively, the electrically insulative material **214** may be directly against an upper surface of semiconductor material (for instance, monocrystalline silicon) of base **212** in some embodiments.

The electrically insulative material **214** may comprise any suitable composition or combination of compositions, and may, for example, comprise one or more of silicon dioxide, silicon nitride, doped silicate glass (e.g., borophosphosilicate glass, phosphosilicate glass, fluorosilicate glass), etc.

The line **215** of the electrode material **25** is shown extending along a direction within the plane of the cross-section of FIG. **15**.

Referring to FIG. **16**, regions **320** and **322** of the programmable material **300** are formed over electrode material **25**. In some embodiments, a barrier material of the type described above with reference to FIG. **4** (not shown) may be formed over the electrode **25** prior to formation of programmable material **300**. The regions **320** and **322** may comprise any suitable materials, including, for example, any of the materials of the regions **30** and **32** of FIG. **4**, the regions **60** and **62** of FIG. **7**, the regions **94** and **96** of FIG. **13**, etc. In some embodiments, the regions **320** and **322** may comprise one or more of the oxygen-containing materials of the systems described above with reference to FIG. **3**. The regions **320** and **322** may be referred to as a first region and a second region respectively, with the second region being formed over the first region. In some embodiments the first region may ultimately correspond to an n-type doped region of a pn diode formed in the "SET" memory state of a memory cell (such as the memory cell **20** of FIG. **4**), and in other embodiments the first region may ultimately correspond to the p-type doped region of such diode. In some embodiments, reservoir mate-

rial analogous to the material **84** of FIGS. **11** and **12** may be incorporated into the programmable material **300**.

Referring to FIG. **17**, the programmable material **300** is patterned into a plurality of spaced-apart memory cell features **216-218**. Such patterning may comprise formation of a photolithographically-patterned mask (not shown), or any other suitable mask (for instance, a mask formed with pitch-multiplication methodologies), over programmable material **300**, followed by a transfer of a pattern from the mask into material **300** with one or more suitable etches, and subsequent removal of the mask to leave the construction shown in FIG. **17**.

Referring to FIG. **18**, electrically insulative material **220** is formed within the spaces between features **216-218**. The electrically insulative material **220** may comprise any suitable composition or combination of compositions, such as, for example, one or more of silicon dioxide, silicon nitride, doped silicate glass, etc.

The electrically insulative material **220** may be formed in the shown configuration by initially forming the electrically insulative material over and between features **216-218**, and then removing the electrically insulative from over the features with a suitable planarization methodology (for instance, chemical-mechanical polishing).

Referring to FIG. **19**, electrode material **27** is formed over the features **216-218** of programmable material **300**, and patterned to form a plurality of lines **231-233**. The lines **231-233** extend along a direction orthogonal to the cross-section of FIG. **19**, and specifically extend in and out of the page relative to the view of FIG. **19**. Accordingly, the lines **231-233** of top electrode material **27** extend substantially orthogonally relative to the line **215** of the bottom electrode material **25**.

The top electrode material **27** may be patterned into the lines **231-233** with any suitable processing, including, for example, utilization of a mask (not shown), one or more suitable etches to transfer a pattern from the mask into material **27**, and subsequent removal of the mask to leave the construction shown in FIG. **19**. In subsequent processing, electrically insulative material (not shown) may be formed over and between the lines **231-233**.

In the shown embodiment of FIG. **19**, the top electrode material **27** is formed directly against programmable material **300**. In other embodiments, one or more barrier materials (not shown) of the type described above with reference to FIG. **4** may be formed between the top electrode material and the programmable material.

The construction of FIG. **19** may correspond to a portion of a memory array. Specifically, the line **215** may be representative of a first series of access lines that extend along a first direction, and the lines **231-233** may be representative of a second series of access lines that extend along a second direction, and which overlap the first series of access lines. Cross-point memory cells **250**a-c (analogous to the cells discussed above with reference to FIG. **6**) are formed at locations where the second series of access lines overlap the first series of access lines. Such cross-point memory cells having programmable material **300** directly between the access lines of the first series and the access lines of the second series.

The cross-point memory cells may have intrinsic pn diodes in a "SET" memory state, and may correspond to any of the memory cells described above with reference to FIGS. **4**, **7**, **9**, and **11-14**. The pn diode may be oriented with the p-type region as the upper region, or with the n-type region as the upper region. Thus, in some embodiments, the lower region **320** may be n-type in the "SET" memory state, and in other embodiments the upper region **322** may be n-type in the "SET" memory state.

The memory cells discussed above may be incorporated into memory arrays of electronic devices, and such devices may be incorporated into electronic systems. The electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regardless of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

The cross-sectional views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings.

When a structure is referred to above as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

We claim:

1. A method of forming and programming a memory cell, comprising:

forming a first region of a programmable material over and directly against a first access line;

forming a second region of the programmable material over the first region; the first and second regions being compositionally different from one another;

forming a second access line over and directly against the second region;

wherein the programmable material has two distinguishable and interchangeable memory states, with one of the states being a "SET" state and the other being a "RESET" state; the "SET" state passing greater current than the "RESET" state when an electrical field is applied across the programmable material; the "SET" and "RESET" states being interchanged with one another by altering one or both of a concentration of ions and a concentration of ion vacancies in at least one of the first and second regions;

wherein the first region is of a first conductivity type in the "SET" state and the second region is of a second conductivity type in the "SET" state, with the second conductivity type being opposite of the first conductivity

type; the first and second regions together comprising a pn diode in the programmable material in the "SET" state; and

altering the ion concentration and/or the ion vacancy concentration in said at least one of the first and second regions to change the programmable material from one memory state to the other.

2. The method of claim 1 wherein the conductive-type state of the first region is n-type in the "SET" state and the conductivity type of the second region is p-type in the "SET" state.

3. The method of claim 1 wherein the conductive-type state of the first region is p-type in the "SET" state and the conductivity type of the second region is n-type in the "SET" state.

4. The method of claim 1 one of the first and second regions comprises conductively-doped semiconductor material and remains the same conductivity type in both the "SET" and "RESET" states.

5. A method of forming and programming a memory cell, comprising:

forming a first region of a programmable material over and directly against a first access line;

forming a second region of the programmable material over the first region;

forming a second access line over and directly against the second region;

wherein the programmable material has two distinguishable and interchangeable memory states, with one of the memory states being a "SET" state and the other being a "RESET" state; the "SET" state passing greater current than the "RESET" state when an electrical field is applied across the programmable material; the "SET" and "RESET" states being interchanged with one another by altering one or both of a concentration of ions and a concentration of ion vacancies in the second region to reversibly form a filament across the second region;

wherein the first region is of a first conductivity type in the "SET" state and the filament is of a second conductivity type in the "SET" state, with the second conductivity type being opposite of the first conductivity type; the first and second regions together comprising a pn diode in the programmable material in the "SET" state; and

altering the ion concentration and/or the ion vacancy concentration in the second region to change the programmable material from one memory state to the other.

6. A method of forming and programming a memory cell, comprising:

forming a programmable material over a first access line; the programmable material having a first region and a second region;

forming a second access line over the programmable material;

wherein the programmable material has two distinguishable and interchangeable memory states, with one of the memory states being a "SET" state and the other being a "RESET" state; the "SET" state passing greater current than the "RESET" state when an electrical field is applied across the programmable material; the "SET" and "RESET" states being interchanged with one another by modifying one or both of a concentration of ions and a concentration of ion vacancies in the second region to reversibly alter the second region;

wherein the first region is of a first conductivity type in the "SET" state and at least part of the second region is of a second conductivity type in the "SET" state, with the second conductivity type being opposite of the first con-

ductivity type; the first and second regions together comprising a pn diode in the programmable material in the "SET" state; and

modifying the ion concentration and/or the ion vacancy concentration in the second region to change the programmable material from one memory state to the other.

7. The method of claim **1** wherein the altering alters the concentration of the ions in at least one of the first and second regions.

8. The method of claim **1** wherein the altering alters the concentration of the ion vacancies in at least one of the first and second regions.

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